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Modeling and Measuring Large Signal PDN Crosstalk and Ground Bounce with a Multi-Phase VRM System Using a Fast Multi-Domain BGA Step Load

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Abstract

Modern AI and datacenter systems, equipped with complex multi-domain Power Distribution Networks (PDNs), grapple with substantial challenges stemming from large-signal crosstalk and ground bounce. These issues are particularly prevalent under fast, dynamic, multi-domain step loads. Such transient conditions, caused by significant current fluctuations on one PDN, can induce considerable voltage noise on neighboring power rails due to mutual electromagnetic coupling. Concurrently, rapid high-current switching within multi-phase Voltage Regulator Modules (VRMs) can generate substantial ground bounce in parasitic return paths. Both of these phenomena degrade power integrity, adversely affecting sensitive on-die circuits and the VRM's transient response.

This work presents a rigorous investigation into modeling and measuring these challenging large-signal phenomena. This paper details a comprehensive approach to model and measure these critical large-signal effects, leveraging full-wave electromagnetic (EM) simulations for accurate parasitic extraction. These extractions are then integrated into transient circuit co-simulations with behavioral VRM models capable of handling large current swings. Our methodology further incorporates precise probing techniques and experimental validation to isolate and quantify induced noise and ground bounce. The ultimate goal is to optimize PDN stability, mitigate unwanted noise, and enhance overall system performance in high-performance digital environments.

Author Biographies

Benjamin Dannan, founder and Chief Technologist at Signal Edge Solutions, is a leading expert in signal and power integrity (SI/PI). As a Keysight ADS Certified Expert, he specializes in advanced packaging for high-performance ASICs, chiplets, and complex FPGAs, utilizing high-speed simulation and 3D EM solutions. He's also proficient with various test and measurement tools, including oscilloscopes and VNAs.

A senior IEEE member with diverse engineering and military experience, Benjamin has designed and launched products ranging from radars to robotic platforms. His expertise spans high-speed circuits, multi-layered PCB design, and EMC product development, ensuring global product compliance. He models complex SoC designs and chiplets at multi-GHz frequencies.

Benjamin holds a BSEE from Purdue, an M.Eng from Penn State, and a cybersecurity certification. A decorated USAF veteran, he served as an Electronic Warfare Officer on 47 combat missions and as a Cyber Operations Officer. He's the DesignCon 2025 Engineer of the Year and a two-time recipient of the prestigious DesignCon Best Paper award.

Heidi Barnes is a Senior Application Engineer for High-Speed Digital applications in the EDA Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and frequency domain simulators to solve power integrity challenges. Author of over 20 papers on SI and PI and recipient of the DesignCon 2017 Engineer of the Year. She is currently a co-chair for the IEEE EPS Electronic Design Modeling and Simulation (EDMS) sub-committee. Experience includes 11 years with Keysight SI and PI EDA software, 6 years designing ATE test fixtures for Verigy, 6 years in RF/Microwave microcircuit packaging for Agilent Technologies, and 10 years with NASA in the

Information Classification: General aerospace industry. Heidi graduated in 1986 with a BSEE from the California Institute of Technology.

Steve Sandler has been involved with power system engineering for more than 50 years. Steve is the founder of PICOTEST.com, a Company specializing in power integrity solutions, including measurement products, services, and training. He frequently lectures and leads workshops internationally on the topics of power, PDN, and distributed systems and is a Keysight-certified expert for EDA software. Steve frequently writes articles and books related to power supply and PDN performance, and his latest book, Power Integrity Using ADS, was published by Faraday Press in 2019. Steve founded AEi Systems, a well-established leader in worst-case circuit analysis and troubleshooting of high-reliability systems.

Will McCaffrey is a Digital Hardware Manager at Northrop Grumman Mission Systems, specializing in high-performance digital board design, signal integrity, and power integrity. He earned his B.S. in Electrical Engineering from the Rochester Institute of Technology and an M.S. in Electrical Engineering from Johns Hopkins University. Will's engineering work spans space-grade interconnects, high-density, high-speed digital circuit boards for aerospace applications, and advanced power integrity modeling for application-specific integrated circuits (ASICs). He has contributed to peer-reviewed publications in the Signal Integrity Journal and DesignCon, where he also received the DesignCon 2025 “40 Under 40” Engineer award as a next-generation leader and innovator.

Tyler Huddleston is a Senior Signal and Power Integrity Engineer at Signal Edge Solutions. He specializes in signal integrity and power integrity modeling and measurement, with a diverse background in developing high-speed digital hardware, firmware, and embedded software for aerospace and defense systems. He holds an M.S. in Electrical and Computer Engineering from Johns Hopkins University, along with a B.S. in Electrical Engineering and a B.A. in Fine Arts from the University of Nevada, Las Vegas.

Emily Tann is a Signal and Power Integrity Engineer with Signal Edge Solutions, where she specializes in optimizing system-level performance and reliability through signal integrity and power integrity measurement and modeling. Prior to her current role, she was with Northrop Grumman, where she contributed to high-complexity projects involving signal and power integrity challenges in mission-critical systems, with a focus on meeting stringent industry standards and design requirements. Emily holds a B.S. in Electrical Engineering with a concentration in Power Systems from the University of Maryland, College Park. Her professional interests include high-speed digital design, power delivery network modeling, and the development of methodologies to ensure compliance with evolving performance and regulatory specifications.

Idan Ben Ezra is a Senior Hardware and PI engineer at Broadcom Semiconductors, CSG-Switch Products group, in SJ, US. In Broadcom, Idan is a focal point in the full system Power Delivery Network analysis and design stages. Developing PI co-simulations and automation flow to cover corner cases (together & separate) for Board (from VRM), Socket, Package & Interposer (Die with HBMs) - IR drop, PDN & Time domain transient response simulation. Idan has hands-on experience with lab power measurements, including correlation to simulation. In the past, he worked at Valens, where he was instrumental as a board designer and as a simulation engineer for high-speed automotive chips. Idan holds a Practical & a Bachelor's (honors) in Electronics and Computer Engineering from HIT, Israel.

I. INTRODUCTION AND BACKGROUND

The rapid pace of technology advancement, largely due to HPC, including AI and Data Center applications, has many of us focused on power performance. Power integrity (PI) engineers are faced with delivering 1000's of Amps over ultra-low micro ohm impedance power delivery networks that are not easy to measure and complex to simulate.

This paper will focus on the power integrity challenge of crosstalk and ground bounce related performance when there is a high current aggressor power rail powering a digital ball grid array (BGA) load. As chip currents are increasing, package sizes are decreasing, meaning that the sensitive circuits, such as transceivers and PLLs, are forced closer to the strong magnetic fields caused by the high di/dt core power rail current. The goal is to correlate the measurement and simulation of these crosstalk and ground bounce effects.

For the purpose of this paper, the Picotest S50 Rev 3 crosstalk demo board will be used. This version of the S50 includes a multi-MCU controller for multi-domain support, clock synchronization, and a BGA attached Picotest S2000-style high-speed GaN load stepper. The design was fabricated with two different printed circuit board (PCB) stack-ups, a 6-layer (6L) and an 8-layer (8L). To enable simulation to measurement correlation, an array of test points is available for assessing both crosstalk and ground bounce at different locations within the package and BGA footprint area. The end goal is to provide a workflow that enables accurate simulation-to-measurement correlation. Measuring micro-ohms and millivolts in a BGA area is evident, and we'll share proposed probing solutions. Simulation complexity can easily mask the ability to troubleshoot crosstalk and ground bounce noise problems, and here, solutions will be provided to simplify the test setups for crosstalk and ground bounce. Measurement validates simulation, and simulation probes where measurement cannot. Together, they create end-to-end digital twin simulations that can solve power delivery crosstalk and ground bounce noise problems.

II. STATEMENT OF THE PROBLEM

Context and Emerging Challenges in High-Performance Systems

Modern Artificial Intelligence (AI) and hyperscale data center systems are characterized by custom Application-Specific Integrated Circuits (ASICs) and advanced packaging solutions, such as UCIe chiplets, that integrate dozens of distinct, high-current power domains onto a single package and PCB. This architecture results in Power Distribution Networks (PDNs) of unparalleled density and complexity. The escalating current demands and the proliferation of power rails require routing structures—including vias, traces, and planes—that are in close physical proximity, inherently increasing mutual electromagnetic (EM) coupling.

The Critical Gaps: Unaddressed Large-Signal Transient Effects

Under fast, dynamic, multi-domain step loads—the characteristic operational state of modern digital systems—two phenomena pose significant degradation to PI performance that are not adequately addressed by conventional small-signal analysis:

1. Large-signal PDN Crosstalk: Significant, rapid current fluctuations on an *aggressor* PDN induce substantial voltage noise onto neighboring *victim* power rails via mutual electromagnetic coupling. This large-signal noise directly violates the tight voltage tolerance requirements of sensitive on-die circuits and complicates the VRM's transient response.
2. Ground Bounce in Return Paths: Concurrently, the rapid, high-current switching characteristic of multi-phase Voltage Regulator Modules (VRMs) generates considerable ground bounce in the parasitic return paths. This ground bounce further degrades the reference voltage stability across all coupled domains.

The Need for a Comprehensive, Validated Methodology

The core problem lies in the difficulty of accurately modeling and experimentally validating the complex interplay between large-signal PDN crosstalk and ground bounce in these high-density systems. Existing methodologies often struggle to integrate the necessary level of detail:

- Modeling Deficiency: Accurately predicting these transient effects requires rigorous, full-wave electromagnetic (EM) parasitic extraction integrated into transient circuit co-simulations with behavioral VRM models that can reliably handle large current swings. Many current tools or methodologies lack this combined fidelity.
- Measurement Deficiency: Isolating and quantifying the separate contributions of coupled noise and ground bounce from multiple aggressors under non-ideal, high-speed transient conditions is challenging and requires specialized measurement techniques and custom hardware.

Therefore, this work seeks to address the fundamental need for a comprehensive methodology to accurately characterize, model, and quantify the impacts of large-signal PDN crosstalk and ground bounce in high-density, multi-rail power distribution networks. Validated with a set of experiments on functioning hardware, this measurement and simulation methodology will ensure system stability, enhance transient response, and meet the stringent power integrity requirements of next-generation AI and datacenter hardware**.**

III. Distinguishing Crosstalk from Ground Bounce Noise Mechanisms

Two primary noise mechanisms corrupting system performance are crosstalk and ground bounce. While ground bounce is intrinsically linked to power integrity and is the canonical example of Simultaneous Switching Noise (SSN), crosstalk represents a separate coupling phenomenon. This paper focuses on separating and quantifying these two distinct noise sources, which is critical for accurate SI/PI analysis.

Crosstalk is defined as the unwanted transfer of energy between adjacent conductive paths, net to net, in a PCB layout. It is an internal electromagnetic coupling phenomenon resulting from the capacitive and inductive coupling between an active line (the aggressor) and a quiescent or passive line (the victim). This coupling is a function of the mutual capacitance (Cm) and mutual inductance (Lm) inherent to the parallel conductor structures and their respective return loops. The victim conductive path can be a signal net (a traditional Signal Integrity, SI, concern), power/ground nets (a significant Power Integrity, PI, concern), or any combination of these. Since Power Delivery Network (PDN) interconnects are generally the largest

conducting structures in a PCB, package (PKG), or die (ASIC), and carry the highest aggregate currents, crosstalk is a pervasive noise mechanism that must be analyzed across the entire system hierarchy [1].

Ground bounce is a distinct form of switching noise that manifests as a voltage fluctuation in the return path (ground or power reference plane) [2]. It is noise coupling on the same shared reference net. It is primarily driven by the total inductance of the return path and by high di/dt caused by system transients, such as laser diodes, RF transmitters, lamp turn-on, or multiple simultaneous switching outputs (SSOs). Multiple SSOs are one possible source of ground bounce, but there are many, even those unrelated to the ASIC. When the top switch in a voltage regulator turns on, high-speed current flows through the output capacitance (Coss) of the lower switch, and when the top switch turns off, the inductor discharges through the lower switch. This can easily create a ground bounce [1].

The physical "ground" is not an equipotential plane, but rather a mesh of parasitic inductive terms distributed across the die, package L_{PKG}, and board L_{PCB}. Ground bounce occurs when a rapid change in current di/dt from an aggressor flows through the total inductance Lret of its local return path. This generates a noise voltage according to Vnoise = L_{ret}* di/dt.

The critical concept is that this ground potential fluctuation is localized to the inductive path carrying the transient current. A bounce generated by the die current may be absorbed by nearby package decoupling capacitance, meaning the die may see an elevated ground potential, while the package and PCB remain relatively quiet.

The noise is introduced because the aggressor current effectively elevates the local return path potential (a specific section of the ground or power plane), thereby shifting the voltage reference for all circuits connected to that specific region. This localized shift is how logic errors occur:

- If a transmitting device's local ground bounces high, its output logic 'Low' level will be elevated.
- If this elevated 'Low' exceeds the input low-level threshold VIL of a non-bounced receiver, the receiver will incorrectly interpret the signal, causing a functional failure.

The fundamental difference lies in **the path and mechanism of noise transfer**:

Table 1 - Mechanisms of Crosstalk and Ground Bounce Noise Transfer

Feature	Crosstalk	Ground Bounce
Primary Mechanism	Direct **net-to-net** capacitive and inductive coupling.	Inductive voltage drop L*di/dt in a **shared return path**.
Coupling Path	PDN → PDN PDN → Signal (Aggressor net to Victim net).	Same net shared return path.
Dependency	Depends on physical proximity and parallelism of signal lines.	Depends on the shared return path inductance interacting with the return path aggressor di/dt.
Noise Type	E and H field coupling, which is often radiated from inductive elements and capacitive elements.	Shifting of the local **voltage reference** between two or more points (ground or power).

The total noise corrupting a signal is a combination of these and other noise sources (such as power rail voltage ripple). Isolating and quantifying these individual noise components is essential as noise margins continue to diminish. This paper details the measurement and simulation methodologies to independently quantify crosstalk and ground bounce, allowing for a comparative analysis of their relative impact on signal integrity and demonstrating that, in some configurations, ground bounce may be significantly less dominant than net-to-net coupling. This analysis will help establish a clear picture of the noise environment, though the full complexity of noise integration and potential transient effects, such as rogue waves, will be left for future exploration.

Analyzing Combined Noise and Measurement Error

When combining all noise sources—crosstalk, ground bounce, and PDN voltage ripple—the total noise becomes complex to isolate and analyze. Furthermore, any quantitative claim is limited by experimental conditions:

- **Measurement Error:** It is essential to first characterize our **measurement error** and the uncertainty in the experimental setup, as the mechanisms for measuring these mV to uV level noise sources differ.
- **Combined Noise Complexity:** When we integrate all of this noise, it becomes very complicated to show that a specific noise component exists or dominates. For instance, showing the potential for extreme, non-linear events like **rogue waves** is an open idea that this paper will leave for future research.

This paper will help readers realize that multiple noise sources exist; our focus is to show how path-to-path noise coupling exists (crosstalk results) and how shared return path noise exists (ground bounce results), and highlight the difference between these noise sources.

Background: Device Under Test and Experimental Platform

The Experimental Platform

The rigorous investigation into large-signal PDN crosstalk and ground bounce necessitates an experimental platform that can accurately emulate the high-density, multi-rail power requirements of modern AI and data center ASICs. The Picotest S50 Rev 3 Crosstalk Demo Board serves as the primary Device Under Test (DUT), designed specifically to facilitate the measurement and isolation of mutual coupling phenomena under dynamic, high-speed load conditions.

The S50 is a multi-layer PCB featuring two electrically independent Power Distribution Networks (PDNs) that interact primarily through close-proximity routing to a dynamic BGA load on the PCB as shown in Figure 1.

Power Domain Configuration

The board provides two distinct, configurable power domains, as shown in Figure 1. These power domains are representative of those found in high-performance digital devices:

- **Aggressor PDN:** A high-current, 4-phase supply designed for up to 100 A output at 0.75V. This domain serves as the primary source of large-signal transient current and subsequent noise induction.
- **Victim PDN:** A lower-current auxiliary 0.85 V supply configured to deliver 15.75 A to the victim load. This domain represents a sensitive power rail or circuit susceptible to coupled noise from the aggressor.

This configuration allows engineers to assess the noise coupling from a high-fluctuation aggressor PDN to a victim PDN or sensitive circuits. Both power supplies can be enabled or disabled independently, facilitating isolation tests to fully characterize the contribution of each power domain to the overall system noise.

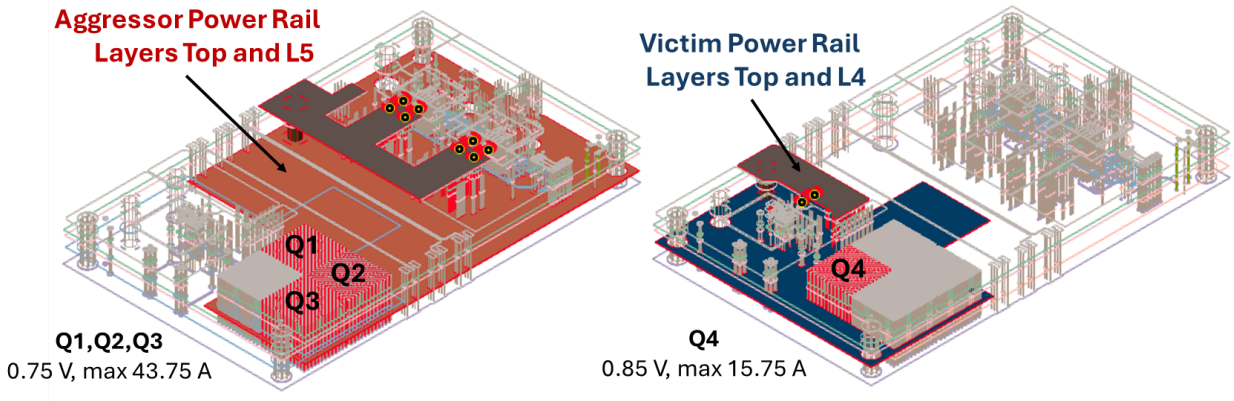


Figure 1 - Aggressor and Victim Power Rails on the 6-Layer S50 PCB

Dynamic Load Excitation System

To generate the challenging transient conditions observed in AI and datacenter workloads, the DUT incorporates a sophisticated, multi-quadrant custom step load. This module connects to both the aggressor and victim PDNs via a 50mm x 50mm BGA footprint, as seen in Figure 4.

Key specifications of the custom step load system include:

- **Edge Rate:** Capable of achieving **sub-nanosecond** rise and fall times, accurately simulating the extremely fast current transients characteristic of modern digital core logic.
- **Independent Digital Control:** The system allows for the development of custom, large-signal excitation waveforms:
    - The Aggressor domain is controlled by **three, independent quadrants** (8-bit control), with a current resolution of 0.25A and a maximum output of 43.75A, and a nominal of 27.75A
    - The Victim domain is controlled by **one independent quadrant** (6-bit control), with a current resolution of 0.25A and a maximum output of 15.75A, a nominal 15.75A.

This highly controllable load enables the precise creation of complex, multi-domain step loads necessary to induce and test the large-signal crosstalk and ground bounce mechanisms.

Parametric PCB Variants

To fully understand the sensitivity of PDN stability and impedance to component selection, the study employs multiple variants of the S50 board:

Table 2 - Variations of the S50 Crosstalk and Ground Bounce PCB

Variant Parameter	Configuration	Purpose of Investigation
Layer Count	6-layer and 8-layer PCBs	To assess the impact of different routing densities and return path configurations on crosstalk and ground bounce magnitude.
Bulk Decoupling	330µF and 470µF Tantalum Capacitors	To understand how bulk capacitor differences impact system stability, impedance, and the damping of transient noise at various excitation frequencies.

The 8-layer version adds two additional ground layers to the stackup. One above and one below the internal victim power layer to help reduce coupling to the aggressor power net. The dielectric thickness between power and ground layers is also reduced to 4 mils on the inner layers to keep the overall stackup at ~64 mils for both the six and eight-layer boards, see Figure 2.

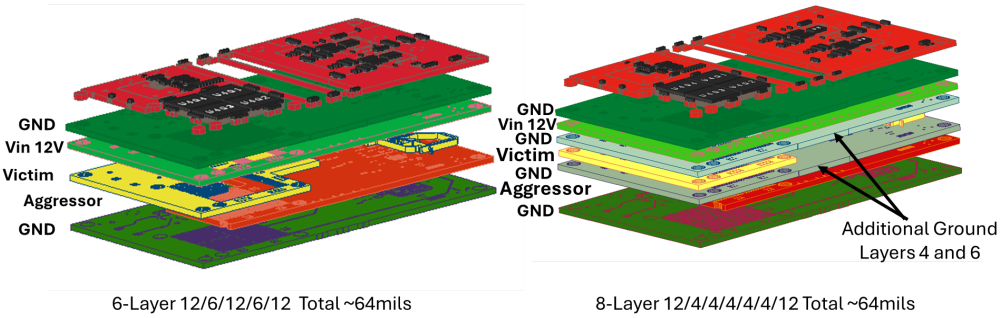


Figure 2 - Stackups of the 6-Layer and 8-Layer Board Configurations

The selection of these bulk capacitors demonstrates that total capacitance is not the sole factor in design; ESR and ESL are equally critical in defining the impedance profile over frequency (see Figure 3). In this application, the 470 µF capacitors achieve a broader bandwidth than the 330 µF alternatives. Specifically, the 470 µF capacitor features an ESR of 4.5 mΩ, which is approximately 25 mΩ lower than that of the 330 µF model. This significantly lower ESR is a necessary requirement for stabilizing the control loop of the aggressor multi-phase LTC7132 voltage regulator; however, a detailed analysis of the impacts these capacitors have on the regulator control loop falls outside the scope of this paper. Additionally for this paper, the focus will be on comparing between the 6-Layer and 8-Layer with the 470 uF capacitors, as the capacitor impedance peak difference between the 330 uF and 470 uF was only at low frequency due to the ESR of the capacitors. This frequency is not the focus of the measurement and simulation, versus the difference between the cost and design properties of the 6-Layer to 8-Layer.

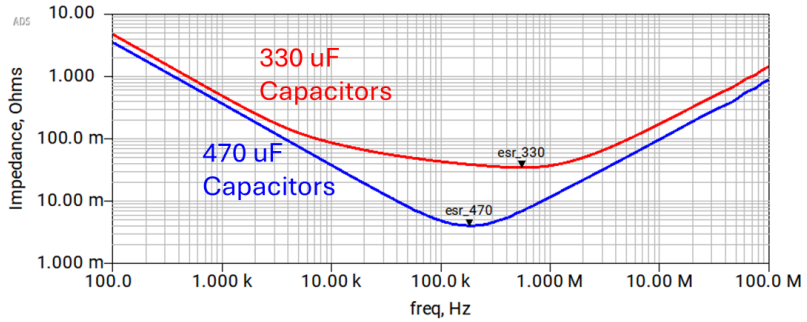


Figure 3 - Measured impedance of the 330 µF Capacitor vs the 440 µF Capacitor

Figure 4 below shows the four (4) test board configurations that were evaluated as part of this effort. The two boards loaded with 330 µF capacitors are labeled as 6L04 and 8L04, and the two with the 470 µF capacitors are 6L01 and 8L02.

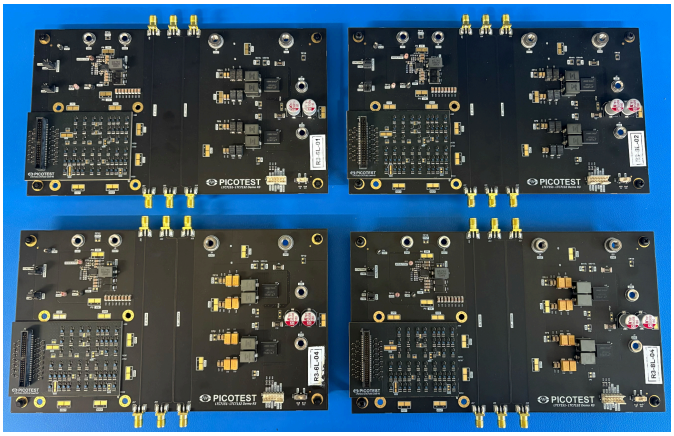


Figure 4 - The four different S50 experiment boards loaded with the dynamic load stepper BGA. Top Left 6L 470 µF, Top Right 8L 470 µF, Bottom Left 6L 330 µF, and Bottom Right 8L 330 µF.

IV. MEASUREMENT SETUP AND TEST WAVEFORMS

Impedance Measurements

The Picotest S50 crosstalk demo board in Figure 5 includes the following test points for impedance measurement. Test points A, B, and Q1.1 are on the Aggressor PDN. Test points C and Q4.D are on the victim PDN. Test points A, B, and C are located on the power PCB for checking the PDN impedance and power supply stability. Test points Q4.D (victim) and Q1.1 (aggressor) are on the BGA load stepper to check the PDN impedance at the load. Additionally, all of these test points can also be used for time domain power rail ripple measurements.

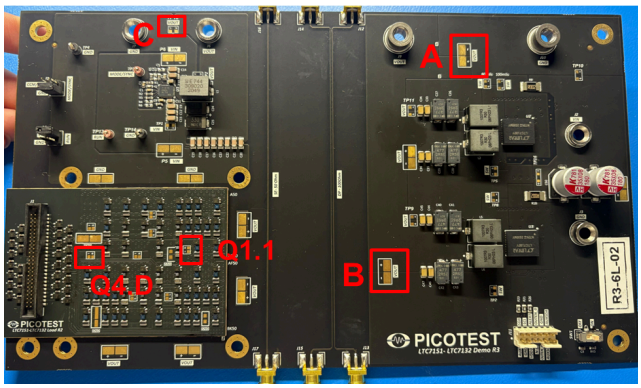


Figure 5 - Impedance measurement test points on the S50 power board with BGA load stepper.

Before performing any time-domain analysis to assess crosstalk or ground bounce, it was important to understand the impedance. Impedance of the load boards was measured using the test setup shown in Figure 6, which included a Bode 500 vector network analyzer, Picotest P2102A 2-Port Probe, Picotest J2113A semi-floating differential amplifier, and a benchtop power supply. Measurements are taken at various points along the board to detect impedance peaks in the PDN. Additionally, this same measurement setup was used to measure each capacitor as part of this PDN, which was then de-embedded from the mount to use for simulation. Together, these measurements help create an accurate EM

simulation model of the as fabricated PCB PDN. Measurement and simulation both correlate to identify PDN impedance peaks in the frequency domain to create worst-case load frequencies for measuring and simulating power rail crosstalk and ground bounce.

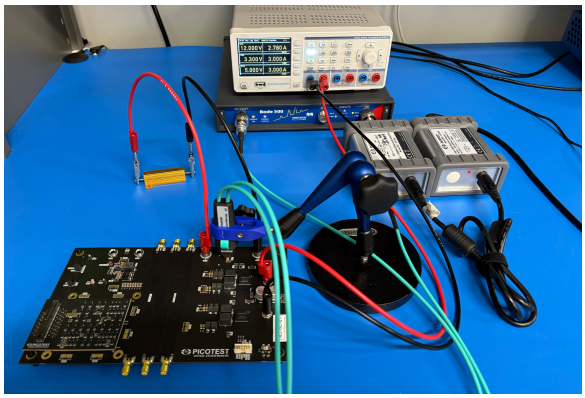


Figure 6 - Two-port shunt impedance measurement setup for measuring ohms to micro-ohms.

As shown in Figures 7 and 8, and summarized in Table 3, measured PDN resonances which occur in the 1-4 MHz range. These are important in order to understand how to excite the forced response on our system during crosstalk and ground bounce measurements, as well as simulation, to achieve the worst-case results.

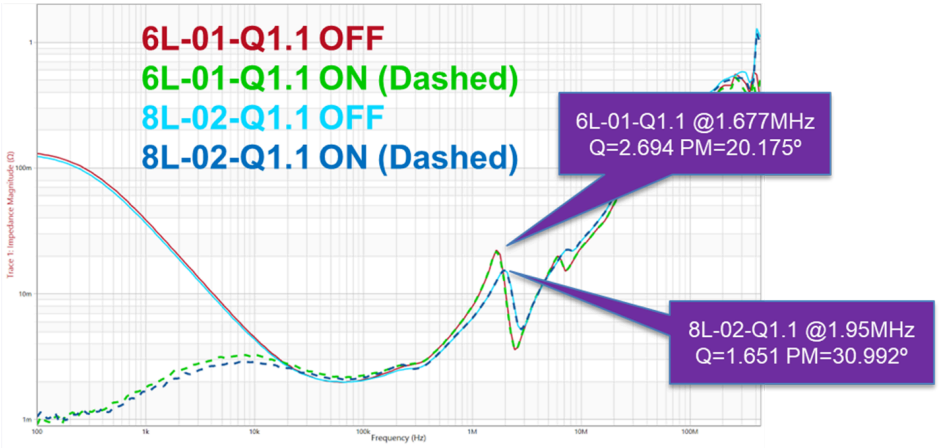


Figure 7 - Impedance Measurement Result at Test point Q1.1 (Aggressor) for 6L-01 and 8L-02, both 470uF boards

Figure 7 compares measurements across two boards, 6L-01 and 8L-02, at measurement point Q1.1 on the aggressor, with the PDN on and off. Both measurements show large impedance spikes at 1.67 MHz and 1.95 MHz. The Q-points for both impedance spikes are over 1.5, indicating instability. These frequency points are what will be excited with a forced response during measurement to determine the worst-case noise on the system. Because the Q-points are seen with the VRM both on and off, the instability seen is due to the PDN's impedance, and not from the VRM.

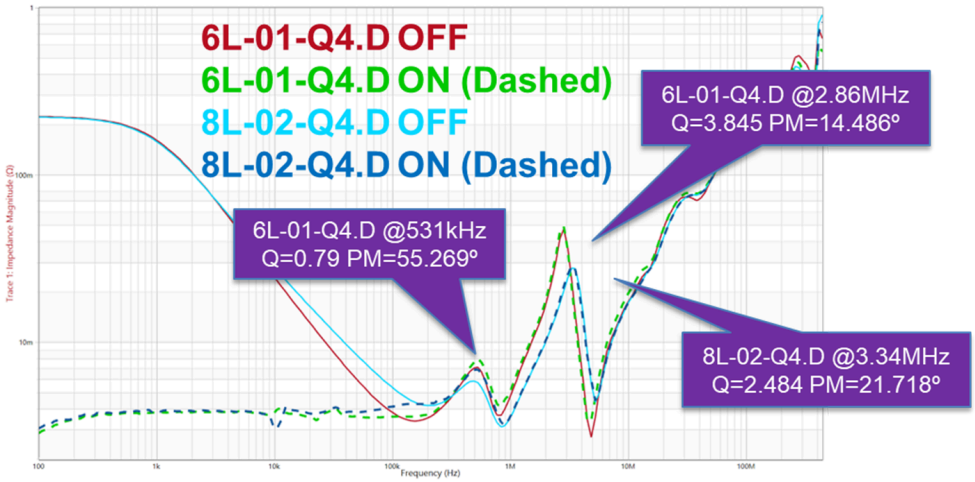


Figure 8 - Impedance Measurement Result at Test point Q4.D (Victim) for 6L-01 and 8L-02

Figure 8 shows the same two boards as Figure 7, but at test point Q4.D on the victim. Here, a third Q-point is seen at 531 kHz. This Q-point has a value of 0.79, significantly less than the Q-points seen at 2.86 MHz for 6L-01 and 3.34 MHz for 8L-02. All three Q-points can be excited to see the impact on the output voltage waveforms.

Table 3 - Impedance Measurement Results: Resonant Q of the Impedance Peak

Impedance Measurement	Q1.1 Agg Q	Q1.1 Agg Freq	Q4.D Vic Q	Q4.D Vic Freq
6 Layer - VRM ON (SN:6L01)	2.70	1.677 MHz	3.85	2.86 MHz
8 Layer - VRM ON (SN:8L02)	1.65	1.95 MHz	2.48	3.34 MHz

To generate the worst-case noise current profiles with this multi-quadrant step load, a custom load controller board, as shown in Figure 9, was developed for this effort. This load controller board houses an Arduino Nano that controls the aggressor and victim GaN FETs to allow for customizable load currents at user-defined frequencies, to stimulate worst-case load current events based on exciting the resonant impedance peaks identified in the PDN impedance measurement.

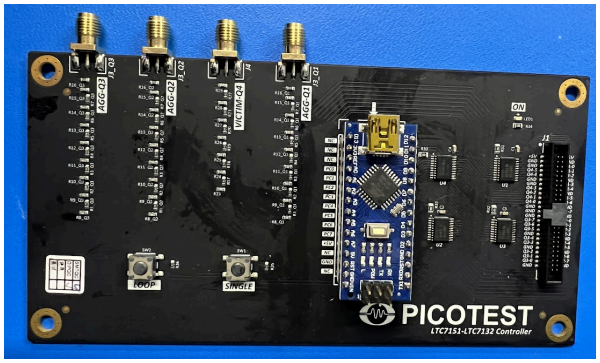


Figure 9 - S50 Single Nano load controller board

The load board uses a push button with software to enable debounce, providing a simple way to generate waveforms. When a button is pressed, the code sets the lower four bits of PORTB (PB0-PB3) to 1, thereby selecting which aggressor and victim lines to activate. This allows for various test cases with the aggressor on and the victim not active, and with the aggressor on and the victim active. An active state is engaged when the button is pressed, generating a high-speed square wave burst with 4 sequential writes to the Nano controller.

This write command sets both PC0-PC7 and PD0-PD7 to the specified current load. Immediately after writing high, the code then writes 0x00 to drive them all low. Every waveform edge occurs around 62.5 ns per write, allowing for burst frequencies in the 2 MHz range, to create a forced response that aligns with the impedance peaks seen in the aggressor output impedance measurement. Additional NOP delays can be added to the software code to allow lower burst data frequencies.

This setup has limitations with waveforms and can only run one frequency for both the aggressor and the victim. A second iteration of the controller board, shown in Figure 10, does allow for separate frequencies for the aggressor and victim load. This board uses two Arduino Nanos with their own programming files. For this paper, the victim load was set to switch at 2.28MHz, and the aggressors were set to 761kHz. This was the maximum frequency that could be reached by the Nano for the victim and still allow for the 3rd harmonic of the aggressor switching frequency to equal the victim switching frequency.. The switching regulator was set to 500KHz. This helps to create a complex, but realistic interaction between the aggressor and victim power rails that is able to excite multiple impedance peaks on both the 6-Layer and 8-Layer designs.

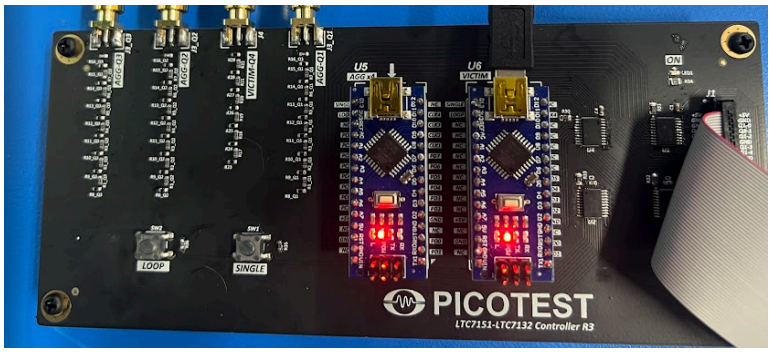


Figure 10 - S50 Dual Nano load controller board Measurement and Validation

The S50 power board with the BGA step loader is designed with dedicated test points across both the aggressor and victim PDNs. These include probe points for measuring Power Supply Rejection Ratio (PSRR) on the high-current PDN, general voltage monitoring, and specific tie-ins to support testing with the transient load stepper solutions. The dedicated probing allows for precise, isolated, and quantifiable measurement of total power rail noise, crosstalk noise, and ground bounce noise, providing the necessary data for experimental validation of the digital twin simulation model with full wave EM model of the PDN co-simulated with dynamic VRM and dynamic sink models.

Ground Bounce Measurements

Test Point Methodology

The Picotest S50 crosstalk demo board (Figure 11) utilizes specific test points to characterize ground bounce—defined as the voltage differential developed between two points on a reference plane due to dynamic current flow. In an ideal system with zero ground bounce, any two points on the ground net remain at the same potential; any measured delta indicates a variation in voltage ripple across the plane.

For this analysis, measurements were focused on several key locations:

- **G1.1 and G1.2:** Located on the power board, these points connect to the BGA load stepper ground pads. While G1.1 is a standard pad, **G1.2** was created by removing the solder mask to measure the differential between the top surface layer and a via deeper in the stackup.
- **G4.L:** Located in the victim quadrant on the top layer of the BGA load stepper.
- **G3.L:** Located in the aggressor quadrant on the top layer of the BGA load stepper.

To accurately identify the locations of aggressors and victims—both of which are influenced by PCB propagation delays—probes were precisely deskewed. Using identical probes and cables ensured that all measurements were aligned along the timing axis, allowing for an accurate correlation between physical location and electrical impact.

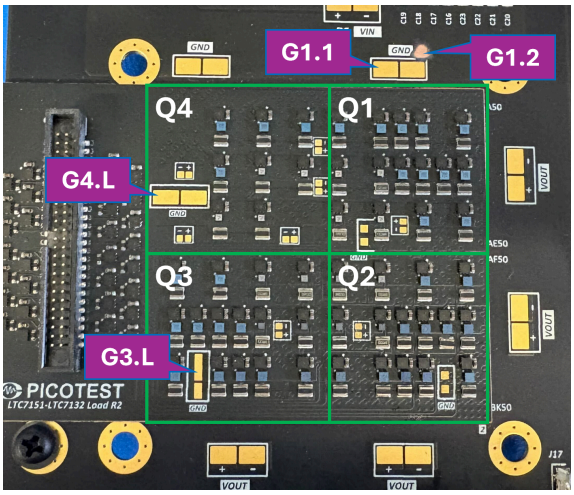


Figure 11 - Ground Bounce Measurement Test Points on DUT

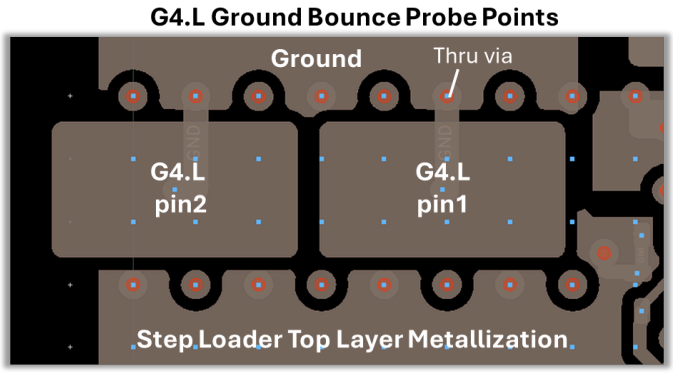


Figure 12 - Ground Bounce Probe Points shown on the step loader PCB CAD data for the top layer.

Probing Challenges and Correlation

While measuring across two points on a reference plane typically suggests a high-CMRR differential probe, standard differential connections often introduce loop area. The resulting exposed probe wires act as antennas, picking up stray magnetic fields generated within the board. To mitigate this, test points were placed adjacent to one another (Figure 12) to minimize loop area while still detecting measurable ground bounce. This high-CMRR probing approach was chosen specifically to ensure the data was suitable for correlation with simulation models.

Measurement Setup and CMRR Validation

Accurate ground bounce characterization requires a high Common-Mode Rejection Ratio (CMRR) to ensure that measured signals reflect actual board behavior rather than measurement artifacts. Because CMRR often varies with frequency, it is a critical factor in high-speed power integrity measurements.

To maximize CMRR, the MXO5 oscilloscope was equipped with an RT-ZISO optically isolated probe (Z101 tip) and a Picotest J2115A coaxial isolator. As shown in Figure 13, this configuration was optimized through iterative testing to minimize the voltage response when the probe was shorted to a single pad during load excitation.

The synergy between these components is vital for high-frequency accuracy. According to Figure 14, the RT-ZISO system provides over 120 dB of CMRR at 1 MHz, while the J2115A provides nearly 90 dB. It should be noted that while an SMA-based connection with the RT-ZISO offers ~25 dB higher CMRR than the Z101 tip, a software limitation on the MXO5 necessitated the use of the Z101 tip for this evaluation.

To establish a baseline for measurement uncertainty, the setup was validated at test point G1.1 with the probe tips shorted to the same probe pad. With both the aggressor and victim currents active to simulate peak load conditions at a 2.28 MHz forced response, the system recorded a baseline uncertainty of 3.63 mVpp (Figure 16). This confirms the high CMRR of the setup under peak operating stress.

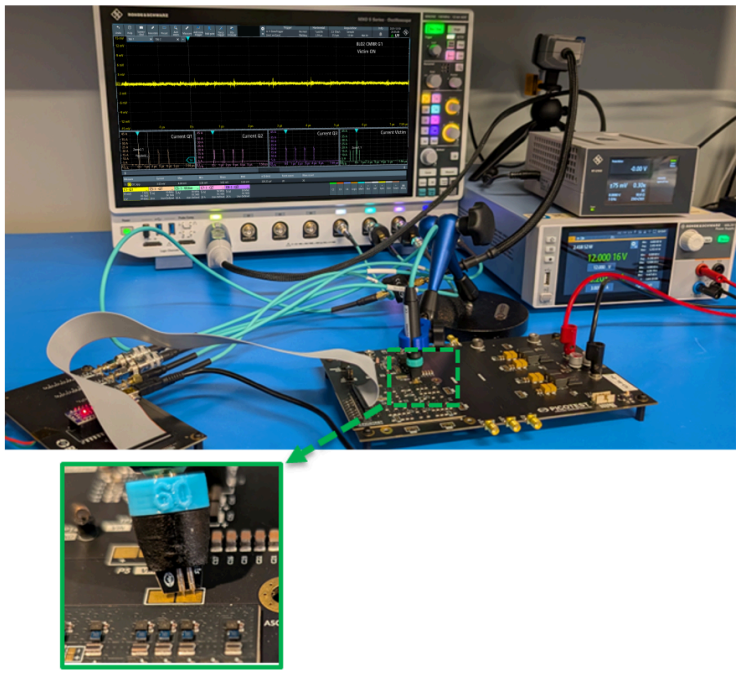


Figure 13 - Ground Bounce Measurement setup with an Isolated Probe shorted to a ground pad for quantifying the measurement uncertainty.

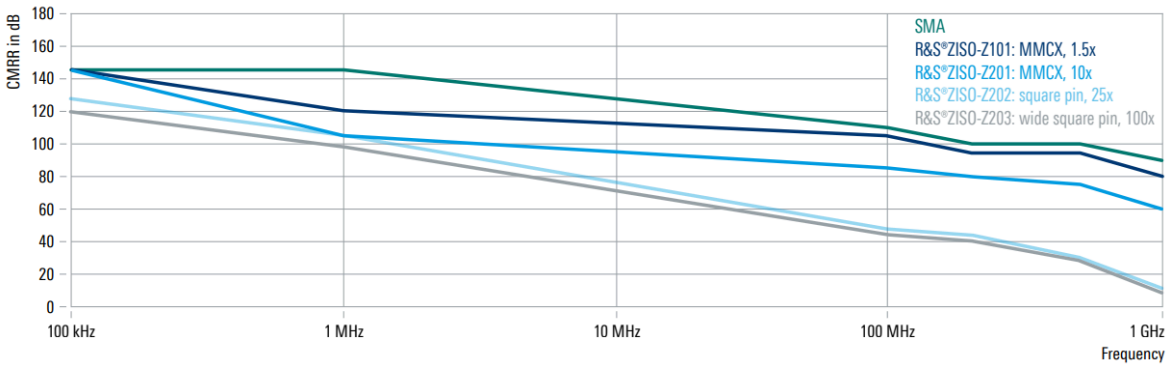


Figure 14 - R&S Probe tip CMRR performance and input voltage derating over Frequency [6]

Figure 15 - Measurement results with shorted probe at G1.1 with Victim current ON and Q1 bit 4 OFF on 8L02 to assess CMRR and measurement uncertainty

Analysis of Ground Bounce Measurements

Based on the data in Table 4 and the waveforms in Figures 16 and 17, the worst-case ground bounce consistently occurs at test point **G3.L** within the aggressor quadrant (Quadrant 3). This peak interference persists regardless of the excitation state of the victim quadrant (Q4), identifying G3.L as the primary point of susceptibility in the system.

For the results shown in Figures 15, 16, and 17, Bit 4 was deactivated on the aggressor quadrants of the Picotest load. This configuration was maintained to ensure the ground bounce results remain consistent with the waveforms used for the crosstalk analysis. A more detailed discussion regarding the function of Bit 4 and the reasoning for its deactivation is provided in the subsequent crosstalk analysis section of this paper.

The peak-to-peak ground-bounce values represent an average of 20 excitation events captured on the MXO5. With the CMRR-optimized setup, the results maintain a maximum measurement uncertainty of approximately **3.6 mVpp**.

Probing Precision and Repeatability

Achieving consistent data required rigorous attention to probe placement and orientation. During the characterization process, it was observed that results varied significantly if the probe angle was not strictly controlled. While a comprehensive study of probing mechanics falls outside the scope of this paper, it is important to emphasize that the integrity of these results relies on high-precision probing. Establishing these strict requirements was essential to minimizing variability and ensuring the repeatability of the data presented under these high-current, 2.28 MHz operating conditions.

Table 4 - Ground Bounce Measurement Results with 2.28 MHz Victim Excitation and 761 kHz Aggressor Excitation

DUT - VIC CURRENT ON	G1.1	G1.2	G3.L	G4.L	Units
6L with 470 µF (SN:6L01)	12.1	8.7	24.9	8.7	Ave mVpp
8L with 470 µF (SN:8L02)	5.9	14.4	24.6	10.7	Ave mVpp
DUT - VIC CURRENT OFF	**G1.1**	**G1.2**	**G3.L**	**G4.L**	**Units**
6L with 470 µF (SN:6L01)	11.7	8.0	24.8	8.3	Ave mVpp
8L with 470 µF (SN:8L02)	5.3	15.4	25.0	9.6	Ave mVpp

Figure 16 - Ground Bounce Measurement Result R3-8L-02 at G3.L with Victim Current OFF and Q1 bit 4 OFF

Figure 17 - Ground Bounce Measurement Result R3-8L-02 at G3.L with Victim Current ON and Q1 bit 4 OFF

Crosstalk Measurements

The Picotest S50 crosstalk demo board shown in Figure 18 shows the following test points used in crosstalk measurements. The lower-left side of the demo board houses the substrate and GaN FETs, which are driven to simulate a load on the PDN. The substrate has four (4) quadrants, labeled Q1, Q2, Q3, and Q4. Q1, Q2, and Q3 are aggressor quadrants, connected to the aggressor power domain, and Q4 is the victim quadrant, connected to the victim power domain. Q4 has 5 test points, labeled A, B, C, D, and E, to provide multiple points for measuring crosstalk induced by the aggressor quadrants. Each of the aggressor quadrants has a single test point to measure the noise.

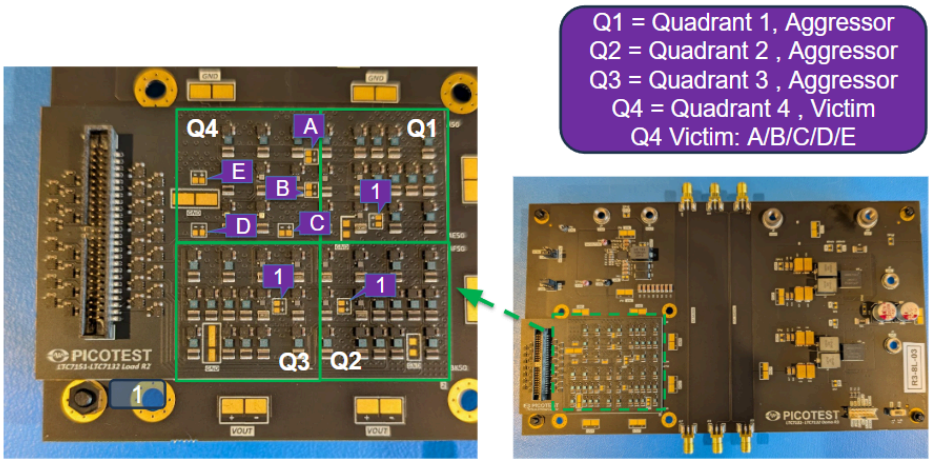


Figure 18 - Crosstalk Measurement Test Points on DUT

To measure crosstalk, all 8 channels on the oscilloscope were used. In addition to minimizing our ground loop measurement error, seven (7) J2115As were used as part of this measurement setup. The results in Table 5 are the peak-to-peak crosstalk measurements averaged across 20 excitation events. The statistical measurements were captured on the MXO5 oscilloscope, where each event is captured at the scope's trigger. Crosstalk was analyzed with the victim's current excitation ON and OFF.

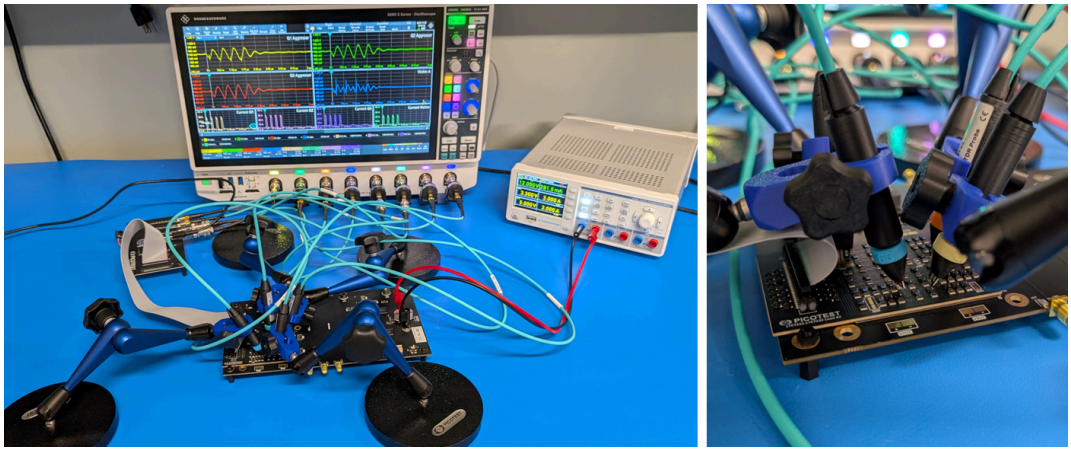


Figure 19 - Crosstalk Measurement Setup

Table 5 - Crosstalk Measurement Results with 2.28 MHz Excitation with all Aggressor Bits Turned ON

DUT - VIC CURRENT ON	Q4-A	Q4-B	Q4-C	Q4-D	Q4-E	Units
6L with 470 µF (SN:6L01)	677.6	306.3	259.4	220.5	280.2	Ave mVpp
8L with 470 µF (SN:8L02)	580.3	265.4	194.3	188.3	205.2	Ave mVpp
DUT - VIC CURRENT OFF	**Q4-A**	**Q4-B**	**Q4-C**	**Q4-D**	**Q4-E**	**Units**
6L with 470 µF (SN:6L01)	158.7	67.9	40.5	41.2	40.2	Ave mVpp
8L with 470 µF (SN:8L02)	133.6	73.5	23.4	26.3	19.4	Ave mVpp

The worst-case crosstalk results across all experimental test cases were consistently found in the 6-layer (6L) board configurations, which are detailed extensively in Appendix A (Victim Current ON) and Appendix B (Victim Current OFF). These appendices provide the definitive data for the maximum coupling observed during this study.

From Table 5, it was observed that crosstalk at test point Q4-A was higher than at all other Q4 test points. This specific peak was traced to Q1 bit 4, which controls a 4-amp cell on the load. To ensure that this high-intensity di/dt was not coupling directly into the probe—thereby skewing the victim rail data—additional measurements were conducted with bit 4 disabled on Q1, Q2, and Q3.

These results, summarized in Table 6, focused on test points Q4-A and Q4-B, as their physical proximity to the coupling bit on the Picotest step load made them most susceptible to measurement artifacts. Our investigation confirmed that the 4A load cell was indeed coupling onto the probe tips. By strategically turning this bit off, we successfully isolated the measurement interference from the true board-level crosstalk. This level of granular hardware troubleshooting allowed us to capture the "clean" worst-case data presented in the Appendices and is a testament to the success of the measurement methodology.

Table 6 - Crosstalk Measurement Results with 2.28 MHz Excitation, and Q1/Q2/Q3 bit4 turned OFF

DUT - VIC CURRENT ON	Q4-A	Q4-B	Q4-C	Q4-D	Q4-E	Units
6L with 470 µF (SN:6L01)	183.3	286.1	187.2	202.2	227.8	Ave mVpp
8L with 470 µF (SN:8L02)	158.1	251.2	171.9	184.5	211.5	Ave mVpp
DUT - VIC CURRENT OFF	**Q4-A**	**Q4-B**	**Q4-C**	**Q4-D**	**Q4-E**	**Units**
6L with 470 µF (SN:6L01)	36.3	65.6	35.9	36.2	36.3	Ave mVpp
8L with 470 µF (SN:8L02)	27.0	60.6	23.3	27.1	21.4	Ave mVpp

V. SIMULATION MODEL SETUP

The simulation goal is to set up a digital twin model that can predict the dynamic time domain crosstalk and ground bounce behavior from the nominal 20.75 Amp per quadrant aggressor power rail to the 15.75 Amp victim power rail. This requires an end-to-end setup with dynamic aggressor and victim loads, aggressor and victim PDNs, and dynamic aggressor and victim switching regulators [3]. The digital twin schematic, shown in Figure 20, can be run with a traditional transient simulator, but this requires long simulation times to reach steady state and makes it difficult to quickly assess large signal behavior. Instead the simulations were done with the Harmonic Balance simulator that simulates in the frequency domain at the fundamental, harmonics, and mixing frequencies of the noise sources to quickly determine steady-state behavior and include large-signal effects.

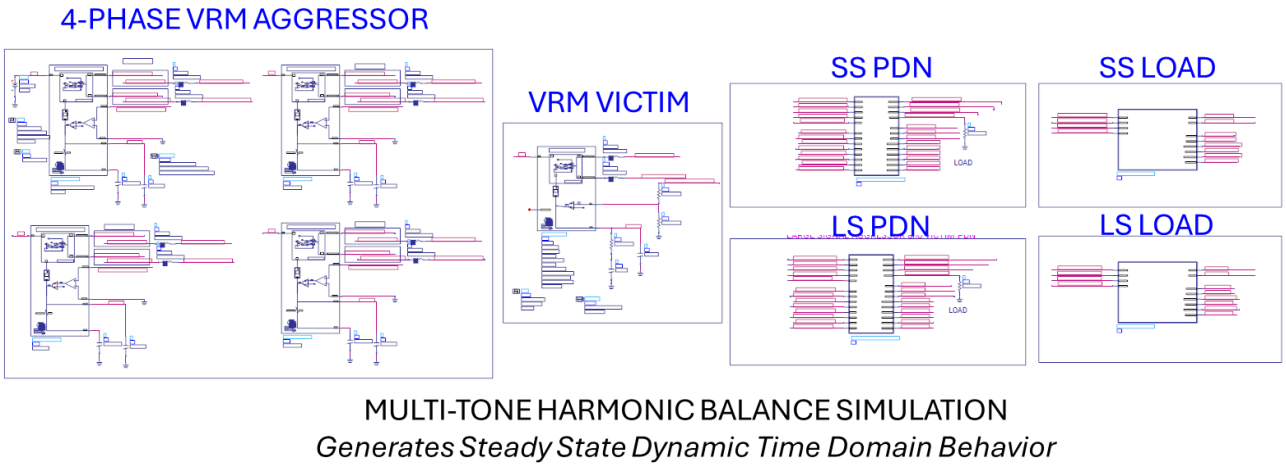


Figure 20 - Simulation Setup for Multi-Tone Harmonic Balance

VRM Modeling Methodology

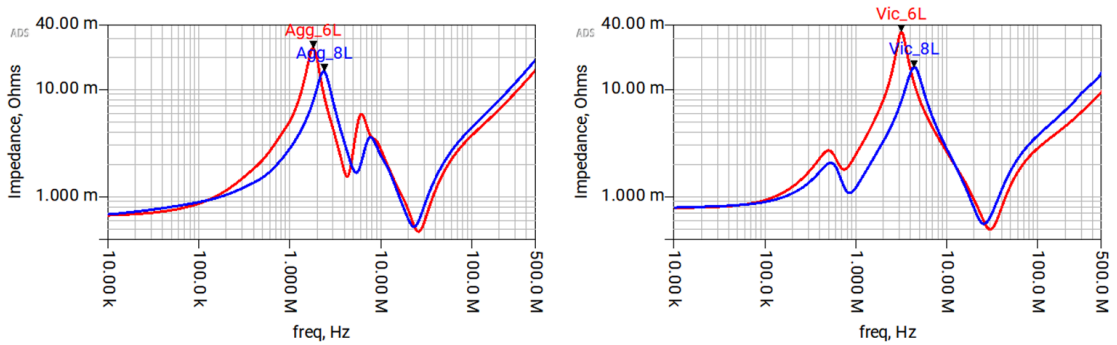
Complete state-space average VRM (SSAM) models for the LTC7132 and LTC7151 were developed using the established Sandler SSAM methodology. This behavioral approach is crucial as it simulates all internal and external noise sources associated with the switched-mode power supply, offering superior predictive accuracy compared to simplified lumped models. The Sandler SSAM is uniquely suited to simulate complex noise sources, such as crosstalk and ground bounce, because its behavioral, state-space formulation captures the dynamic control-loop behavior and both small-signal AC noise and large-signal switching ripple with high fidelity, while providing significantly faster simulation times [4-5].

These SSAMs support comprehensive end-to-end power integrity (PI) simulations, enabling analysis of small-signal ripple and large-signal switching ripple. The models are designed to facilitate rogue wave analysis, target impedance analysis, crosstalk analysis between power domains and sensitive signals, stability analysis, and the design/modeling of the VRM control loop. Furthermore, they are structured to accurately support multiphase designs, including precise simulation of current sharing between phases. The LTC7132 is a dual-output PolyPhase DC/DC synchronous step-down monolithic regulator featuring an I²C-based PMBus compliant serial interface. It utilizes a constant-frequency current mode architecture combined with a unique scheme optimized for exceptional performance in sub-milliohm DCR applications. The LTC7151S is a high-efficiency monolithic synchronous buck regulator capable of delivering up to 15.75A to the load. To reduce the number of frequencies required in the Harmonic Balance simulation it was decided to set the VRM switching frequency to 500kHz for both the aggressor and victim.

PCB PDN Modeling Methodology

The requirement to assess net-to-net cross talk coupling vs. same-net ground bounce from an aggressor power rail to a victim net dictates that the EM setup must be able to consider both differential and common mode effects. Typical EM simulations make use of the PCB ground layers to define the reference return in the EM port setup, but this only allows for a total differential noise between the power rail and the ground rail. To look at the noise ripple on the power rail separate from the ground return net, it is necessary for the EM simulator to add an isolated ground plate reference below the PCB. This is similar to how conducted EMI measurements are done by adding an isolated ground plate below the electrical unit under test. In simulation this allows a pin port to be placed on any power, ground, or signal net at any location to measure the ripple voltage relative to the isolated ground plate layer. The total differential noise between a power net and a ground net at a test point is simply the subtraction of the ripple voltage on the ground net from that of the power net.

Before connecting the PDN model in the end-to-end digital twin schematic, it is important to verify with some simple impedance measurements that the simulation setup is correct and has the required fidelity to capture the resonances of interest. Correlating with measurements, with reference to the simulated PDN impedances in Figure 21, we see that the 6-layer board has a peak impedance that is more than double that of the 8-layer board, both for the Aggressor PDN and the Victim PDN. The lower inductance of the added ground layers on the 8-Layer board is what brings the peak impedance down, while at the same time shifting the resonance to a higher frequency. This behavior is seen in both the simulated and measured data.



1.8 MHz, 2.4 MHz 3.2 MHz, 4.3 MHz

Figure 21 - Simulated Impedance of the 6 Layer and 8 Layer Aggressor and Victim PDNs

Dynamic Load Modeling Methodology

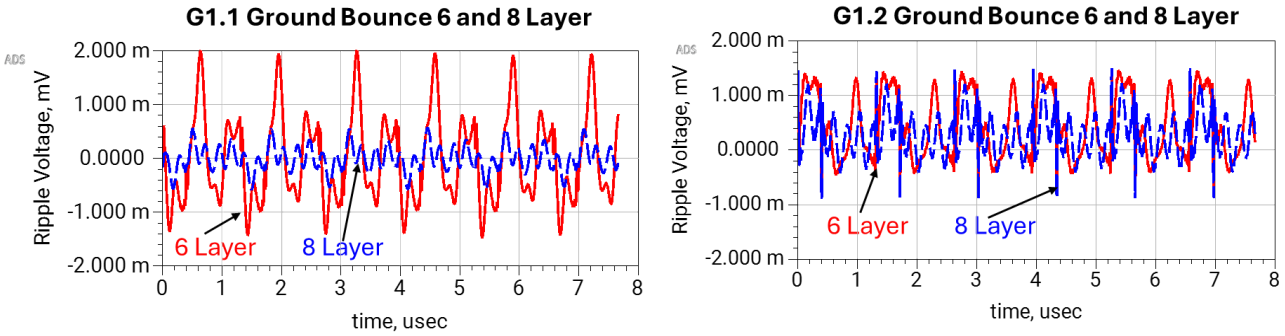
The dynamic load makes use of the same resistive style switch that is used for the large signal behavior of the VRM upper and lower switches. The single switch has an effective rise and fall time to provide a smooth transition from the on to off state. The custom Picotest step-loader has 45 aggressor load cells and 8 victim load cells that can deliver a wide range of dynamic loads. The simulation digital twin is also capable of running the aggressor dynamic load at the same or different frequency from the victim dynamic load.

To look for worst case crosstalk, and compare the improvement seen by going from the 6-layer PCB to the 8-Layer PCB with more ground planes, the dynamic load switching frequencies were selected to target the impedance peaks from 700 MHz and 5 MHz for the Victim. In the case of the ground bounce measurements the Aggressor was set to 761 kHz and the Victim was set at the 3rd harmonic of the Aggressor equal to 2.28 MHz. The Harmonic Balance simulator is still the simulator of choice for its ability to handle multiple tones with their intermodulation while still reducing simulation times down to a few minutes for steady state time domain results.

VI. RESULTS AND ANALYSIS

The measurements for ground bounce are challenging in that the measurement probe plus and minus connections must remain close in order to avoid large loop inductances in the measurement. This prevents the use of a quiet ground further away from the location where ground bounce is to be measured. In simulation, it is still a challenge to minimize the port inductance, but the addition of a reference ground plate directly below the PCB is much better than what can be achieved in measurement. However, to mimic the ground bounce measurement, the simulation is set up to calculate the differential noise across the adjacent ground pads that are the same as used in the measurement. To make the measurement more realistic, the regulators are set to be switching at 500 kHz, the aggressor is switching at 761 kHz, and the victim is switching at 2.28 MHz. This does make it more challenging to get exact simulation to measurement correlation in terms of the phase between the different excitations and sensitivities of high Q resonances to fabrication tolerances which can create large signal effects and rogue waves. However, there is significant value in a digital twin that demonstrates the same trends and can be used for design exploration to identify what features are controlling performance and cost.

The interesting data is to compare simulation and measurement for the G1.1 and G1.2 locations. The G1.1 probe pads are connected to two of the top layer ground pads at the BGA that then use vias to drop down to the internal ground layers. The G1.2 probe pads use one of the BGA top layer ground pads, and another adjacent ground location on the top layer. Figure 22 shows the expected simulation result that is also supported by measurement that the added grounds of the 8 Layer board reduces the localized ground bounce between adjacent BGA ground pads. However, the data for the BGA ground pad relative to the adjacent top layer ground actually shows a slight increase in noise. Tabular data is also included to show the trends that agree with measurement, including the Victim G4.L location. The G4.L location inside the step loader board near the switching die does not see a significant difference between the 6 layer and 8 layer boards.



Simulated DUT - VIC CURRENT ON	G1.1	G1.2	G4.L	Units
6L with 470 µF	3.5	2.0	1.3	mVpp
8L with 470 µF	1.1	2.2	1.2	mVpp
Simulated DUT - VIC CURRENT OFF	**G1.1**	**G1.2**	**G4.L**	**Units**
6L with 470 µF	2.5	2.0	1.4	mVpp
8L with 470 µF	0.6	2.3	1.3	mVpp

Figure 22 - Simulated Ground Bounce at Locations G1.1 and G1.2

The simulated data for ground bounce does result in an overall lower magnitude than measurement, but this is to be expected. The simulator has a much lower noise floor and must always trade-off simulation fidelity with resources and time. The key difference here is using harmonic balance to simulate in less than 2 minutes for steady state time domain behavior at the switching frequencies, while in measurement a burst of 4 pulses was used to avoid thermal issues and reduce data set sizes.

The measured ground bounce data does not provide any spatial information, but in simulation it is easy to look inside the PCB at how the ground currents are flowing on each layer as shown in Figure 23. This data shows the current densities for the aggressor load switching at 761 kHz and the victim turned off. The 6-Layer design has a significant amount of the current on the outside bottom layer which can result in radiated EMI. The 8 Layer PCB concentrates most of the aggressor ground currents from Layer 2 and the Bottom Layer to the inner Layer 6 GND.

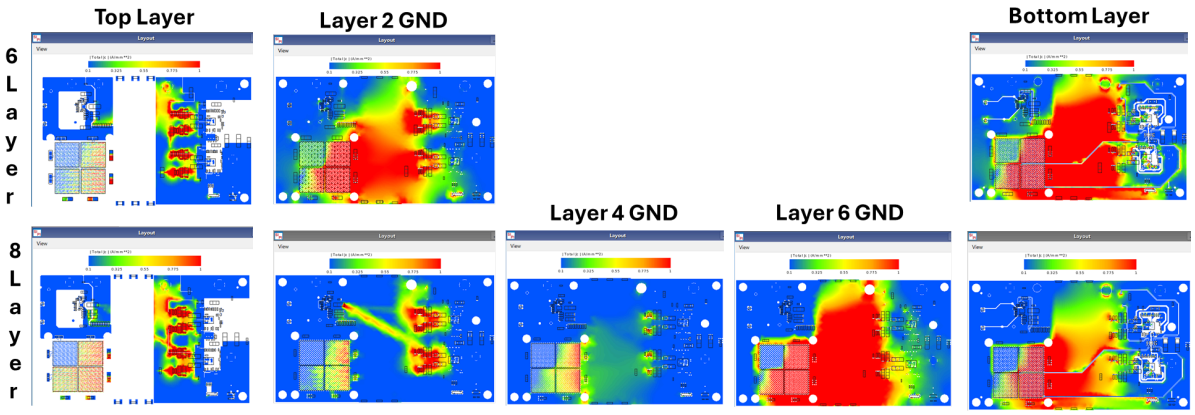
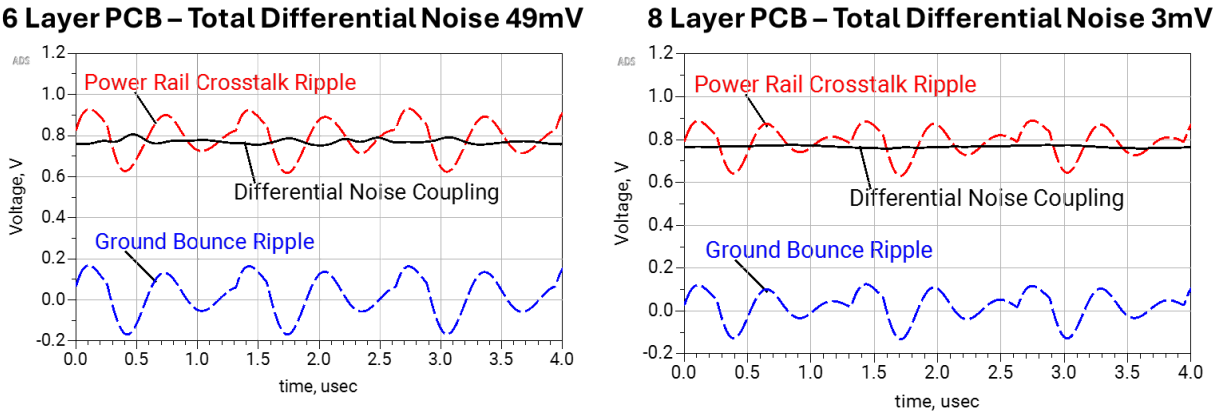


Figure 23 - Current Density plots at the Aggressor 761 kHz from the ADS PIPro EM simulator.

The next source of EMI to look at is the net to net crosstalk coupling that can occur between the Aggressor power rail and the Victim power rail. The dynamic loads are again set to 761kHz for the Aggressor and 2.28 MHz for the Victim. The crosstalk measurements can only look at differential voltage ripple, but in simulation it is possible to look at the voltage ripple separately on the power rail and the ground rail as shown in Figure 24. The data clearly shows how noise coupling can cause both the power and the ground of the victim net to move up and down, but it is the difference between the power and ground rail that result in the differential noise ripple. The simulation results for peak to peak crosstalk ripple from the Aggressor to the Victim power rail correlate with measurement and confirm the benefits of the two additional ground layers in the 8-layer stackup. The 6-layer and the 8-layer have similar peak-to-peak noise coupling on the victim power net but on the 6-layer the noise on the ground rail is slightly larger resulting in more noise on the 6-layer design. Also, the noise ripple on the 8-layer board is more symmetric between the power and ground rails resulting in better cancellation of the crosstalk and less differential noise ripple.



Simulated DUT - VIC CURRENT ON	Q4-D
6L with 470 µF (SN:6L01)	221
8L with 470 µF (SN:8L02)	141

Simulated DUT - VIC CURRENT OFF	Q4-D
6L with 470 µF (SN:6L01)	49
8L with 470 µF (SN:8L02)	3

Figure 24 - Simulated Noise on the Victim Power Nets of the 6-Layer and 8-Layer Boards

Plotting the current density from the EM simulator can also provide valuable insights into where the noise coupling is occurring and how to improve the layout to mitigate EMI. The plots in Figure 25 show the coupling from the Aggressor at 2.28 MHz while the Victim is turned off. The higher coupling on the 6 layer board occurs at sharp corners in the layout. The ground return is more complicated to understand since there are multiple layers involved for both the 6-Layer and 8-Layer designs, however, by looking at the ground closest to the victim we can clearly see that the 6-layer design will have more ground bounce.

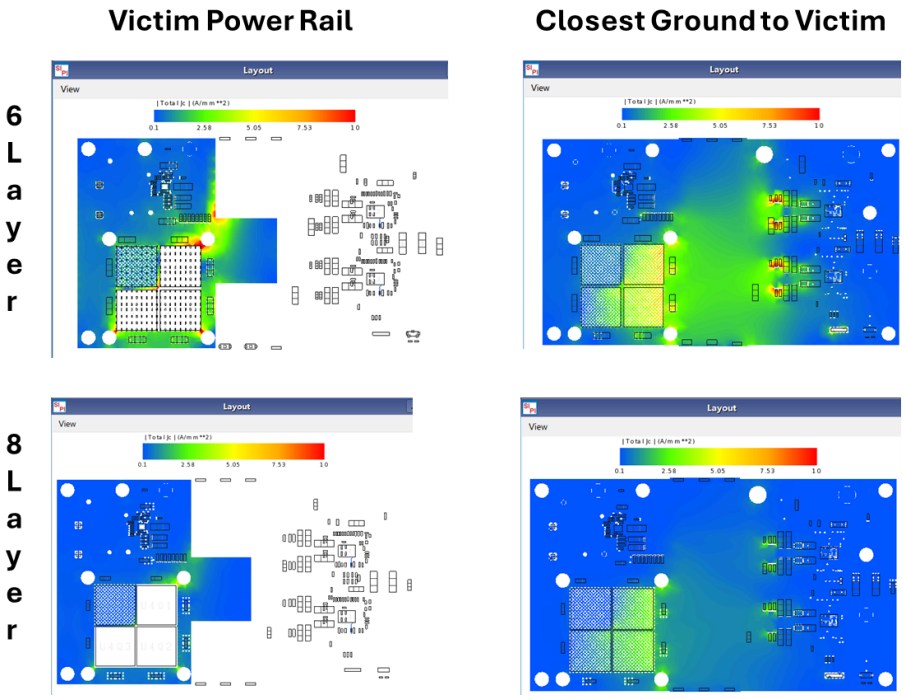


Figure 25 - Current density plots showing net to net crosstalk from the Aggressor to the Victim at 2.28 MHz with the Victim turned off.

Further investigation is needed, but it looks like the removal of the Victim power rail from looping around the BGA along with the removal of sharp corners in the path of the Aggressor currents could significantly improve the 6-Layer design and potentially achieve similar performance to the 8-Layer at a lower cost.

VII. CONCLUSIONS AND SUMMARY

This paper successfully demonstrates a robust methodology for measuring and modeling crosstalk and ground bounce in high di/dt environments, effectively bridging the gap between theoretical simulation and physical hardware. We consider the results of this effort a definitive victory in Power Integrity (PI) engineering, as we navigated extreme difficulties in synchronizing digital twin simulations with real-world hardware.

The success of this work is highlighted by the exceptional correlation achieved across multiple test cases. Specifically, for crosstalk at Q4-D, we achieved a peak-to-peak voltage correlation within **0.5 mVpp** on the 6-layer board (with 470 µF caps) and within **47 mVpp** on the 8-layer board with victim current active. Furthermore, our ground bounce results showed a delta of less than **8 mVpp** between measurement and

simulation. Given the sensitivity of these environments, these positive trends represent a major milestone in predictive modeling.

These results were made possible by overcoming critical physical challenges. We identified that probe placement, angle, and orientation are paramount for repeatability. By utilizing an isolated probe with high Common-Mode Rejection Ratio (CMRR) and specialized isolation stages, we achieved a **3 mV** measurement uncertainty, successfully neutralizing common-mode noise that typically masks these margins.

The key technical takeaways include:

- **The Power of Symmetry:** The 8-layer board's advantage lies in its symmetric coupling environment, allowing noise to move in tandem for significant differential cancellation.
- **Resonant Frequency Risks:** We identified a critical impedance peak near 2 MHz where the 6-layer board's impedance was more than double that of the 8-layer design.
- **Layout over Layer Count:** Field analysis revealed that routing victim rails around aggressors and sharp corners was the primary coupling mechanism, suggesting that layout optimization can sometimes outperform raw layer count.

Future Work

Building on this success, future research will expand into EMI simulation and measurement correlation. We will investigate how higher intensity di/dt on the bottom layer impacts radiated emissions, specifically comparing 6-layer versus 8-layer designs to quantify EMI reduction benefits. Additionally, we will focus on modeling and measuring crosstalk within voltage regulator sense lines to further refine high-precision feedback loop integrity.

VIII. ACKNOWLEDGEMENTS

A special thanks to Bertin Soto for his support in the PCB layout of these test fixtures, which made this paper possible.

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X. APPENDIX: WORST-CASE CROSSTALK ANALYSIS

The 6-layer board configurations consistently yielded the worst-case crosstalk results across all test cases. This reinforces the findings that the lack of symmetry and reduced ground planes in the 6L design significantly heighten coupling risks.

- Appendix A: Worst-Case Crosstalk Amongst All Test Cases (R3-6L-01 with Victim Current ON and Q1 bit 4 ON)
- Appendix B: Worst-Case Crosstalk Amongst Test Cases With Victim Excitation Turned Off (R3-6L-01 with Victim Current OFF and Q1 bit 4 ON)

Appendix A - Worst-Case Crosstalk Amongst All Test Cases (R3-6L-01 with Victim Current ON and Q1 bit 4 ON)

Appendix B - Worst-Case Crosstalk Amongst Test Cases With Victim Excitation Turned Off (R3-6L-01 with Victim Current OFF and Q1 bit 4 ON)