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Methods to Model and Measure Noise Mitigation with Embedded Capacitors in High Current PDNs for AI and Cloud Compute

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Abstract

The rapid growth in Data Centers, AI, and supercomputing demands significantly faster edge rates at the package and PCB levels, necessitating superior power delivery network (PDN) solutions. While traditional VRMs and bulk capacitors dominate at lower frequencies, the impact and effectiveness of embedded capacitors in high-current PDNs remain critical for achieving high performance. This paper explores various embedded capacitor technologies and their layout considerations within PCB and package stackups. Through detailed simulation and measurement, we analyze the influence of embedded capacitors on system performance, noise reduction, and power delivery efficiency in AI/datacenter applications. We specifically investigate how embedded capacitors impact large signal phenomena, validating findings through both measurements and simulation, and present methods for effectively modeling small signal analysis with these components. We also discuss manufacturing challenges and examine the impact of lateral versus vertical power delivery systems; specifically, we address how vertical power, while more efficient and higher performance due to proximity to the chip, removes the ability to place backside decoupling. This work provides comprehensive insights into leveraging embedded capacitors to optimize PDN design for next-generation ASICs.

Author Biographies

Benjamin Dannan, founder and Chief Technologist at Signal Edge Solutions, is a leading expert in signal and power integrity (SI/PI). As a Keysight ADS Certified Expert, he specializes in advanced packaging for high-performance ASICs, chiplets, and complex FPGAs, utilizing high-speed simulation and 3D EM solutions. He's also proficient with various test and measurement tools, including oscilloscopes and VNAs.

A senior IEEE member with diverse engineering and military experience, Benjamin has designed and launched products ranging from radars to robotic platforms. His expertise spans high-speed circuits, multi-layered PCB design, and EMC product development, ensuring global product compliance. He models complex SoC designs and chiplets at multi-GHz frequencies.

Benjamin holds a BSEE from Purdue, an M.Eng from Penn State, and a cybersecurity certification. A decorated USAF veteran, he served as an Electronic Warfare Officer on 47 combat missions and as a Cyber Operations Officer. He's the DesignCon 2025 Engineer of the Year and a two-time recipient of the prestigious DesignCon Best Paper award.

Tyler Huddleston is a Senior Signal and Power Integrity Engineer at Signal Edge Solutions. He specializes in signal integrity and power integrity modeling and measurement, with a diverse background in developing high-speed digital hardware, firmware, and embedded software for aerospace and defense systems. He is a Keysight Certified Expert and holds an M.S. in Electrical and Computer Engineering from Johns Hopkins University, along with a B.S. in Electrical Engineering and a B.A. in Fine Arts from the University of Nevada, Las Vegas. He was also recognized as a DesignCon 2026 40 Under 40 Engineer.

Steve Sandler has been involved with power system engineering for more than 40 years. Steve is the founder of PICOTEST.com, a Company specializing in power integrity solutions, including measurement products, services, and training. He frequently lectures and leads workshops internationally on the topics of power, PDN, and distributed systems and is a Keysight-certified expert for EDA software. Steve frequently writes articles

and books related to power supply and PDN performance, and his latest book, Power Integrity Using ADS, was published by Faraday Press in 2019. Steve founded AEi Systems, a well-established leader in worst-case circuit analysis and troubleshooting of high-reliability systems.

Heidi Barnes is a Senior Application Engineer for High-Speed Digital applications in the EDA Group of Keysight Technologies. Her recent activities include the application of electromagnetic, transient, and frequency domain simulators to solve power integrity challenges. Author of over 20 papers on SI and PI and recipient of the DesignCon 2017 Engineer of the Year. Experience includes 11 years with Keysight SI and PI EDA software, 6 years designing ATE test fixtures for Verigy, 6 years in RF/Microwave microcircuit packaging for Agilent Technologies, and 10 years with NASA in the Information Classification: General aerospace industry. Heidi graduated in 1986 with a BSEE from the California Institute of Technology.

Vedashree Chaphekar is a Senior Engineer at Qnity Electronics Silicon Valley Technology Center. She specializes in RF design, signal and power integrity analysis, and the prototyping of advanced electronic materials for high-frequency, high-speed digital systems. Vedashree also develops EMI mitigation solutions using absorbers, board-level shields, and magnetic components to reduce electromagnetic interference in consumer electronics and data center applications. She holds a Master's degree in Electrical Engineering from NC State University. Prior to her current role, Vedashree worked as an RF R&D Engineer at Amphenol Antenna Solutions, where she focused on prototyping, designing, and testing base station antennas for major wireless providers.

Kalyan Rapolu is a Senior Solutions Engineer for High-Speed Digital applications at Keysight Technologies' EDA Group. He specializes in Signal and Power Integrity application development, leveraging Keysight ADS for advanced modeling and simulation. Previously, he served as Principal Engineer at the DuPont Silicon Valley Technology Center, leading R&D in PCB and IC packaging materials for high-frequency, high-speed systems. With over a decade of experience spanning RF design, SI/PI analysis, and advanced material characterization, Kalyan bridges materials science and system-level performance to enable next-generation electronics. He holds a Ph.D. and M.S. in Electrical Engineering from Villanova University and has also worked at Applied Materials as a Senior Process Engineer.

In addition to his industry contributions, Kalyan is a passionate educator, currently teaching at UCSC Silicon Valley Extension, where he shares his expertise in signal and power integrity with the next generation of engineers.

Emily Tann is a Signal and Power Integrity Engineer with Signal Edge Solutions, where she specializes in optimizing system-level performance and reliability through signal integrity and power integrity measurement and modeling. Prior to her current role, she was with Northrop Grumman, where she contributed to high-complexity projects involving signal and power integrity challenges in mission-critical systems, with a focus on meeting stringent industry standards and design requirements. Emily holds a B.S. in Electrical Engineering with a concentration in Power Systems from the University of Maryland, College Park. Her professional interests include high-speed digital design, power delivery network modeling, and the development of methodologies to ensure compliance with evolving performance and regulatory specifications.

I. INTRODUCTION AND BACKGROUND

Necessity drives innovation. Nowhere is this more evident than in modern ASIC design. As operating frequencies rise and power demands increase, maintaining low impedance across the power delivery network (PDN) becomes critical to keeping rail voltages within tolerance.

At the heart of the challenge lies a simple but powerful relationship, as shown by EQ(1):

$$Z^2 = \frac{L}{C} \tag{1}$$

Here, capacitance (C) and parasitic inductance (L) are bound by the PDN impedance (Z). As rail voltages decrease and currents rise, (Z) must decrease to minimize di/dt voltage ripple. The ratio of L and C in the PDN path must be reduced at a second-order rate to meet this requirement. This exponential drop in impedance requires an increase in capacitance and/or a decrease in inductance to reach this low impedance in the power delivery network.

Since this path cannot be avoided, engineers must work with the available parameters:

- **Parasitic inductance (L):** from capacitors and planes
- **Capacitance (C):** from decoupling capacitors and planes

This equation has fueled intense R&D into advanced capacitor technologies, including embedded solutions to increase C while simultaneously reducing L. The goals are clear:

- Reduce the path inductance, including the loop inductance to SMT capacitors.
- Increase capacitance at the ASIC while minimizing the physical footprint of capacitors.

This paper highlights a solution based on ultra-thin dielectric layers. The thin dielectrics reduce the plane inductance while at the same time increasing the plane capacitance. By simultaneously reducing inductance and increasing capacitance, this technology addresses both sides of the equation. The result can be a step change in PDN performance to reduce voltage noise ripple and a more efficient use of PCB real estate.

a. Background on Thin Capacitor Embedded Laminates

Thin embedded planar capacitance materials play a critical role in modern power distribution networks (PDNs), particularly in high-speed digital systems where signal integrity (SI) and power integrity (PI) are paramount. These materials consist of ultra-thin dielectric layers sandwiched between copper planes, forming a distributed capacitance structure with very low inductance directly within the PCB stack-up. By providing a low-inductance, high-frequency decoupling path, embedded planar capacitance materials significantly reduce power supply and dynamic load power rail voltage ripple, which is essential for maintaining stable operation of high-speed ICs. At first glance, the embedded capacitance is promising with its ability to be located directly at the IC and not requiring any additional board space. However, a closer look shows that the reduction in inductance is just as important, if not more. The answer to whether this added capacitance improves performance is that it depends. Adding nF capacitance with low

inductance at the IC can eliminate small decoupling capacitors and free up board space as long as the PDN impedance is on the order of 100 milliohm or higher. In the case of high current with 1000's of amps, this small nF of plane capacitance is ineffective. However, reducing the plane inductance reduces the path inductance to the decoupling capacitors, thereby increasing their bandwidth and making them more effective. This may be a small impact for a single capacitor, but in high current designs with 100's of decoupling capacitors, this small reduction in path inductance can have a much larger impact on the total impedance of the PDN.

For example, the impedance for a bare PCB with no capacitors shown in Figure 1 below, but with a thin dielectric layer, can only achieve a total embedded capacitance in the nF range; in this case, 3 nF. Combining this with a typical path length results in 55 pH of inductance and a characteristic impedance of 100 mOhms at 300 MHz, where the L and C cross. If a design requires a target impedance lower than 100 mOhms, then the only way to achieve this is to add significant SMT capacitors for the total C and in parallel to reduce the inductance. This shows that the PCB capacitance is static at 3 nF, but the benefit of the lower path inductance is a multiple of the number of capacitors in parallel. A 1000 Amp high di/dt load with 100's of decoupling capacitors can benefit significantly from the lower inductance of a thin dielectric layer between power and ground as close as possible to the decoupling capacitors.

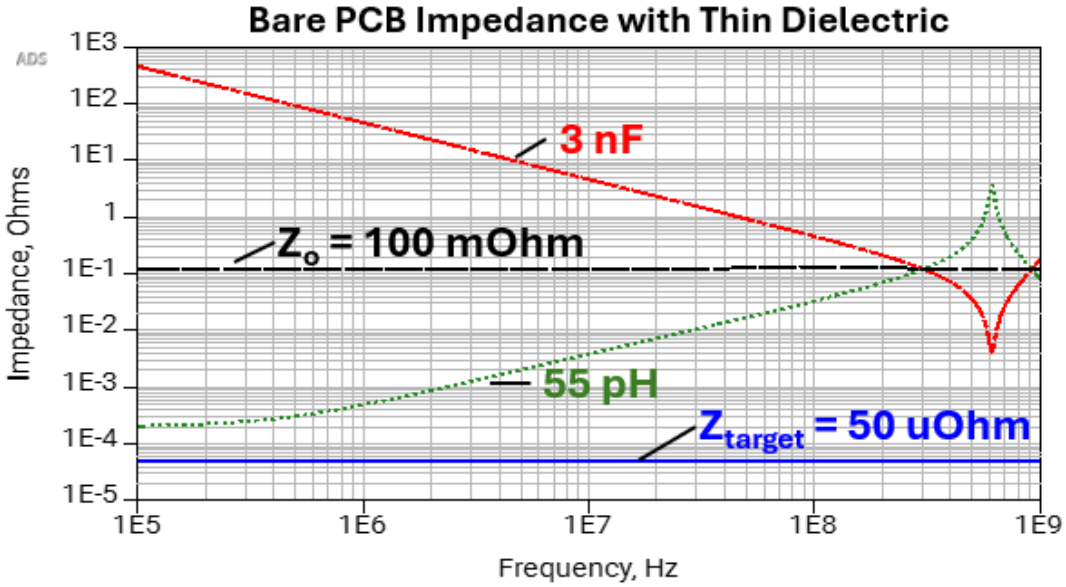


Figure 1 - Bare PCB Impedance with Thin Dielectric

For systems with high-current switching loads such as processors, FPGAs, and ASICs, the allowed voltage ripple margins shrink, and the benefits of embedded planar capacitance materials become even more pronounced. Rapid current transients during switching events can cause substantial voltage fluctuations if the PDN impedance is not tightly controlled. Embedded capacitance layers help flatten the impedance profile, reducing simultaneous switching noise (SSN) and ground bounce, which in turn enhances signal integrity by preventing timing errors and jitter. Additionally, embedded planar capacitance materials contribute to better electromagnetic compatibility (EMC) by suppressing high-frequency noise propagation through the board. As designs push toward higher data rates and lower

supply voltages, integrating thin planar capacitance into the PCB stack-up is a strategic necessity for achieving robust SI/PI performance in advanced electronic systems.

b. Empowering High-Speed AI Systems with Interra® HK04J Embedded Capacitance Thin Laminates

Using thin copper-clad laminates as power/ground plane pairs in multilayer PCBs is an effective approach for improving power integrity, enhancing signal quality, reducing crosstalk and resonance-related radiation, suppressing power-rail noise, and providing greater flexibility in stack-up design. These thin laminates, often referred to as embedded capacitance materials, achieve these benefits by lowering power-plane impedance and reducing PDN loop inductance, thereby supporting the high-frequency decoupling performance required in advanced AI and datacenter systems.

Qnity's Interra® HK04J is an industry-proven embedded capacitance laminate that has been adopted extensively for power/ground plane pairs in multilayer PCBs in high-end networking equipment. The material is halogen-free and features a homogeneous dielectric structure, making it well aligned with standard and high-performance FR-4 manufacturing practices. While its use requires thoughtful stack-up design and some care during board fabrication, Interra® HK04J has shown good compatibility with surrounding materials, enabling reliable performance and consistent yields even in demanding, high-performance PCB builds.

Interra® HK04J is offered in dielectric thicknesses of 1-mil (25 µm nominal) and 0.5-mil (12 µm), using RTF and/or HVLP copper foils in 0.5, 1, 2, and 3 oz copper weights. It is certified to IPC-4821/1. Figure 2 illustrates the typical construction of the thin laminate along with a microsection image of the 1-mil Interra® HK04J structure. The capacitance (C in nF) of the laminate is determined by the common plate area and dielectric thickness and can be calculated by EQ(2) as

$$C\,(nF) \;=\; 0.2247 \;\times\; K \;\times\; \frac{A}{t} \qquad (2)$$

where K is the dielectric constant, A is the common plane area in square inches, and t is the dielectric thickness in mils. Capacitance increases as the dielectric constant increases and/or the dielectric thickness decreases.

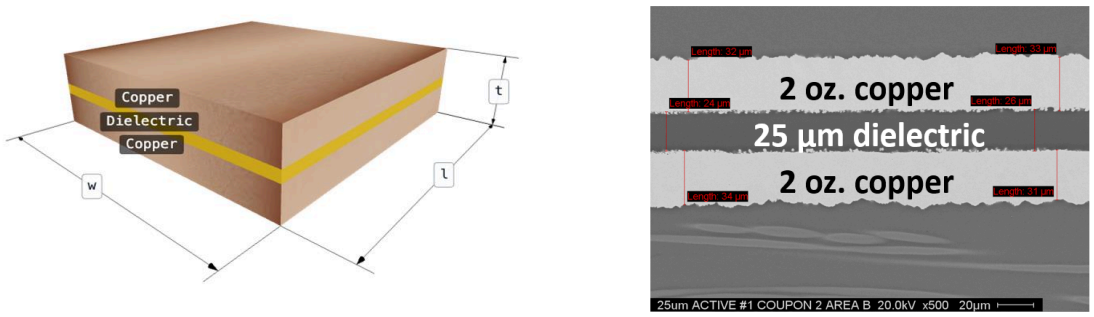


Figure 2 - Typical thin laminate construction (left) and microsection photo of Interra® HK04J (right)

Interra® HK04J provides excellent capacitance stability across frequency and temperature, ensuring that its dielectric constant remains consistent under varying operating conditions. This stability is critical for maintaining high-speed via SI performance in advanced PCB designs. Figure 3 [1] and [2] present the typical capacitance response of Interra® HK04J across frequency and temperature, respectively. These advantages have been discussed in the previous paper [1], which talks about the use of thin laminates in a power distribution system.

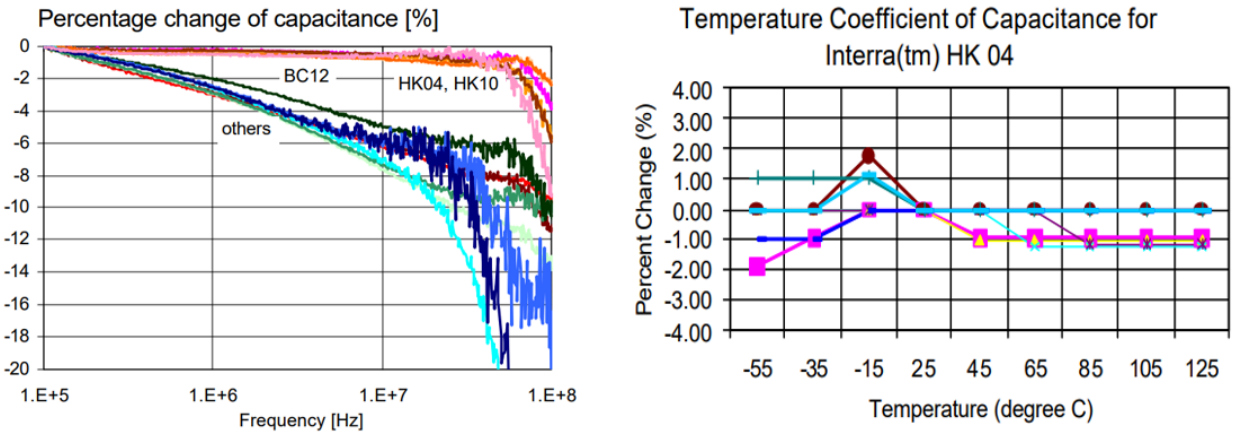


Figure 3 - Capacitance stability of Interra® HK04J over frequency [1] and temperature [2]

The loop inductance for square planes is given by:

$$L_{loop} = \mu \frac{h \times L}{w},$$

where $\boldsymbol{\mu}$ is the magnetic permeability, h is the dielectric height, and L and w are the length and width of the planes. By using thinner materials, the loop inductance is proportionally decreased by the decrease in the height between the power and ground planes.

II. STATEMENT OF THE PROBLEM

Quantifying the benefit of an embedded capacitive material for power delivery networks is very much dependent on the application and constraints that exist when designing the PDN. The focus of this paper is on the challenges of high current, 2000 Amps and above. This type of application requires a significant number of power and ground plane layers when doing lateral power delivery to reduce. The multiple layers are not just for IR drop thermal challenges, but also for achieving ultra-low micro-ohm impedance power delivery to the dynamic digital load across DC to 100's of MHz. Lowering the impedance at high frequencies is done by increasing the capacitance while at the same time reducing the total loop inductance.

Embedded capacitor PCB materials can provide higher capacitance by allowing fabrication of a stack-up with thin materials and/or by increasing the dielectric constant. It was shown that the plane capacitance is not significant for designs that require micro-ohms of PDN impedance, but that the lower loop inductance is critical. This paper will focus the investigation on the benefits of the thin dielectric layer to show how

the decrease in inductance can increase the effective bandwidth of SMT ceramic capacitors at a BGA load to improve the high-frequency decoupling.

III. TEST PLATFORM

The test fixture is shown in Figure 4 and consists of two main components: a Power Board and a Load Board. The Power Board is a PCBA designed to emulate a typical power system for a high-power ASIC, delivering 0.8 V at 2000 A. This design builds upon work established in a previous paper [2], which explored the validation of 2000 A core rails using substitute step-load devices. That study detailed critical design aspects, including the impact of various VRM topologies, the necessity of accurate modeling to predict Power Delivery Network (PDN) impedance, and the role of PCB EM simulations in identifying parasitic reflections. Specifically, those simulations were shown to be essential for optimizing capacitor selection, and particularly for bottom-side, high-frequency decoupling capacitors requiring minimal inductance.

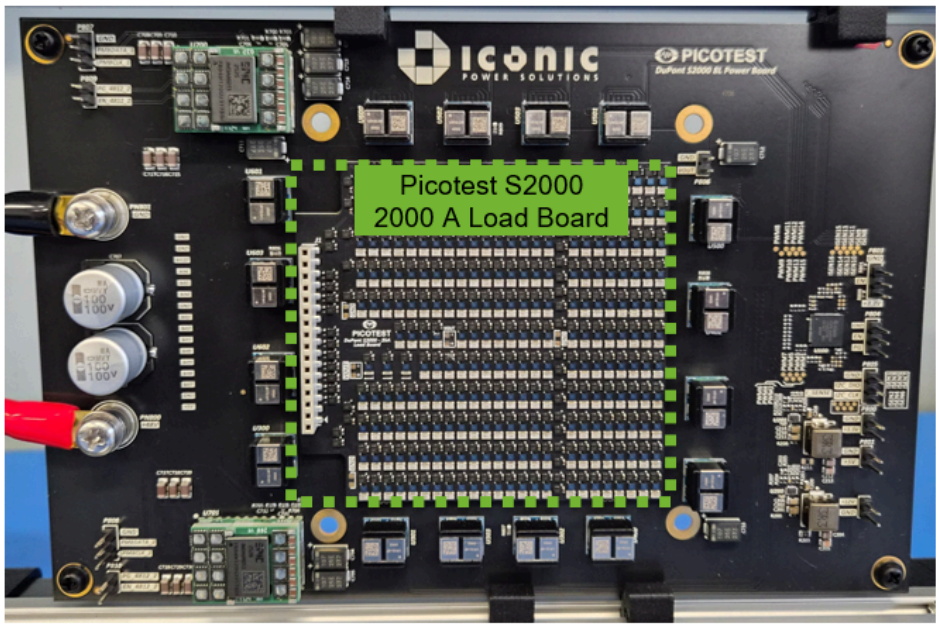


Figure 4 - Test Fixture with Load Board Mounted on Power Board

While the previous work [2] focused on the motherboard-level PDN, this paper shifts focus to the BGA and package interface. The load board utilizes a BGA interposer design to emulate the ASIC load via an array of gallium nitride (GaN) power transistors. These GaN FETs enable realistic sub-nanosecond switching, offering a significant performance leap over silicon (Si). While a standard Si MOSFET regulator typically exhibits edge speeds between 1ns and 30 ns, state-of-the-art GaN switches can be two orders of magnitude faster [3].

Two versions of this test fixture were built and measured: (1) with the 1 mil Interra® HK04J core dielectrics and (2) with more traditional 2 mil S1000-2 core dielectrics. The response to various large current loads were measured to evaluate the performance enhancement with the Interra® HK04J materials.

IV. SIMULATION MODEL SETUP

The primary objective of the simulations was to compare the PDN performance with and without embedded capacitor laminate materials and quantify the benefits of placing a distributed, embedded capacitance at the load. Three core laminate materials were used in the simulation. Their key characteristics are defined in Table 1.

Table 1 - Core Dielectric Material Properties

Core Material	Core Thickness	Dielectric Constant
S1000-2	2 mil	3.7
Interra® HK04J 25 µm	1 mil (25 µm)	3.5
Interra® HK04J 12 µm	0.5 mil (12 µm)	3.5

The dielectric constant of the Interra® HK04J material is in the range of typical PCB materials; the 1 mil and 0.5 mil thickness materials are the novel characteristics of the material. With these reduced thicknesses, the capacitance between adjacent layers is increased, and the inductance is decreased, both of which benefit PI performance.

The stackups of the modeled boards are given in Figure 5. The S1000_2 and Interra® HK04J_25µm stackups are producible lamination buildups developed with the PCB manufacturer. The Interra® HK04J_12µm and Interra® HK04J_12µm_outer are stackups that were only explored by simulation.

Layer	S1000_2	HK04J_25um	HK04J_12um	HK04J_12um_outer
Soldermask		Simulated, Built & Measured	Simulated Only	
Copper				
Prepreg	3.5 mil S1000-2MB	4.0 mil TU-862 HF	4.0 mil TU-862 HF	**0.5 mil Interra® HK04J**
Copper				
Core	2.0 mil S1000-2	**1.0 mil Interra® HK04J**	**0.5 mil Interra® HK04J**	4.0 mil TU-862 HF
Copper				
Prepreg	2.5 mil S1000-2MB	4.0 mil TU-862 HF	4.0 mil TU-862 HF	4.0 mil TU-862 HF
Copper				
Core	2.0 mil S1000-2	**1.0 mil Interra® HK04J**	**0.5 mil Interra® HK04J**	4.0 mil TU-862 HF
Copper				
Prepreg	2.5 mil S1000-2MB	4.0 mil TU-862 HF	4.0 mil TU-862 HF	4.0 mil TU-862 HF
Copper				
Core	2.0 mil S1000-2	**1.0 mil Interra® HK04J**	**0.5 mil Interra® HK04J**	4.0 mil TU-862 HF
Copper				
Prepreg	3.5 mil S1000-2MB	4.0 mil TU-862 HF	4.0 mil TU-862 HF	**0.5 mil Interra® HK04J**
Copper		20% reduction in thickness		
Soldermask				
Total thickness	**51.98 mil**	**39.16 mil**	**37.66 mil**	**41.16 mil**

Figure 5 - Built & Simulated Stackups

In simulation, extracted EM models of the power board and load board were generated for analysis for each of the 4 stackups.

We assessed the impact of solderball parasitics between the power board and load board and found the effect to be negligible on this design with hundreds of solderballs grouped into a single port. An EM extraction of the load board with solderballs modeled showed about 0.04 pH more inductance than without solderballs. To simplify the simulation setup of multiple configurations, we excluded solderball modeling from our study.

a. Simulated Impedance

The simulation of the bare board impedance seen by the load is shown in Figure 6. The impedance of the power board is measured at the grouped BGA pins where the load board would be installed. The impedance of the bare load board is measured at the grouped GaN FET cells. From Figure 6, the impedance provides the capacitance of the bare boards, where Table 2 summarizes these results. As expected, the thinner materials increase the capacitance seen at lower frequencies. An increase in capacitance is seen in both the load and power boards with the Interra® HK04J material embedded in the stackup. Specifically, the power board capacitance increases by 84% with the 25 µm-thick Interra® HK04J material and by 200% with the 12 µm-thick Interra® HK04J material. On the load board, the capacitance increases by more than 243% with the 25 µm-thick Interra® HK04J material and by 500% with the 12 µm-thick Interra® HK04J material.

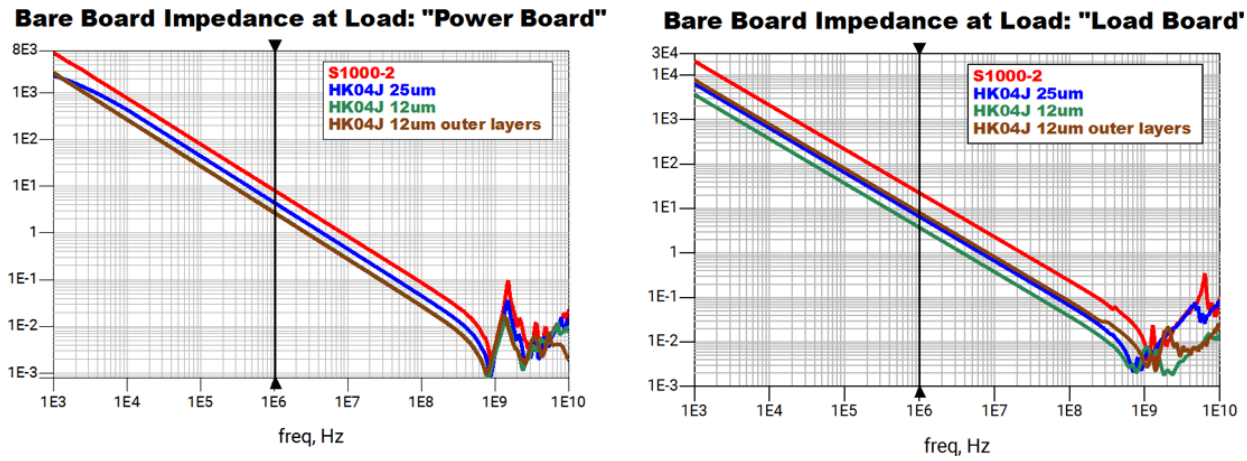


Figure 6 - Simulated Impedance of the Bare Power Board and Bare Load Board

Table 2 - Board Board Capacitances

	S1000_2	**Interra® HK04J_25µm**	**Interra® HK04J_12µm**	**Interra® HK04J_12µm_outer**
Power Board	19 nF	35 nF (+84%)	57 nF (+200%)	58 nF (+205%)
Load Board	7 nF	24 nF (+243%)	42 nF (+500%)	19 nF (+171%)

These increases in capacitances are not enough to decouple our 2000 A load. However, 10s of additional nano-Farads from an embedded capacitor material would be sufficient to reduce the number of discrete capacitors on low power applications of less than 10 W, saving board real-estate and simplifying the BOM. The novel benefit of these ultra-thin dielectrics between the power and ground planes is their performance improvement in the capacitor loop inductance to the load.

Loop inductance from select capacitors identified in Figure 7 was simulated with the 4 stackup variations to assess their performance. The loop inductance path for each of the capacitors is from the capacitor on the power board to the grouped GaN FET cells on the load board. The simulation results for impedance and loop inductance are shown in Figure 8, and a summary of the loop inductances is provided in Table 3.

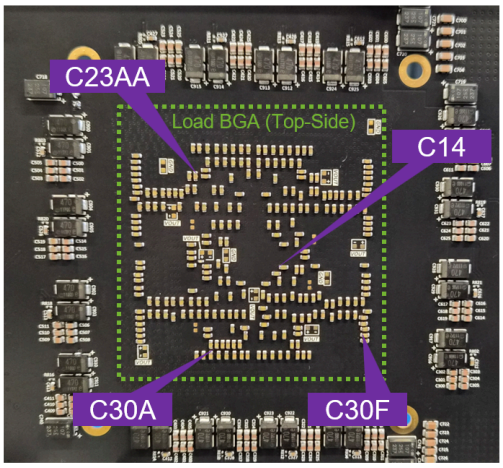
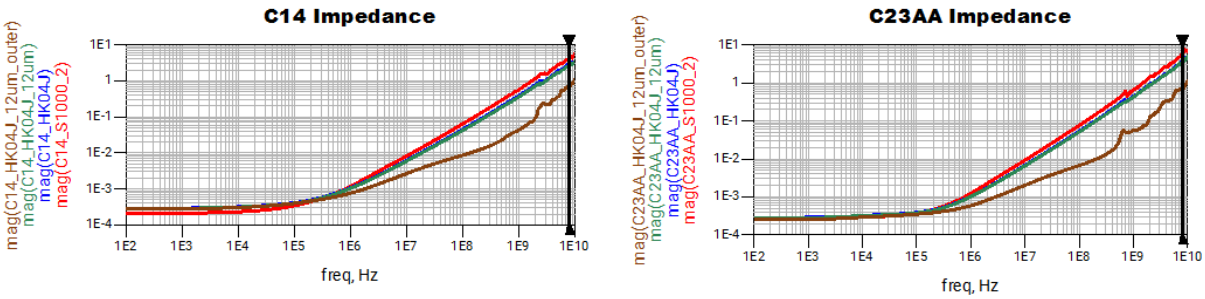


Figure 7 - Loop Inductance Capacitor Measurement Locations on Bottom-Side of the Power Board Directly Below the Load BGA

Table 3 - Loop Inductance from Select Capacitors to Load

	Loop Inductance			
	C14	**C23AA**	**C30A**	**C30F**
S1000_2	89 pH	116 pH	124 pH	105 pH
Interra® HK04J_25µm	54 pH (-39%)	79 pH (-32%)	82 pH (-34%)	67 pH (-36%)
Interra® HK04J_12µm	51 pH (-43%)	73 pH (-37%)	61 pH (-51%)	61 pH (-42%)
Interra® HK04J_12µm_outer	14 pH (-84%)	14 pH (-88%)	12 pH (-90%)	10 pH (-90%)

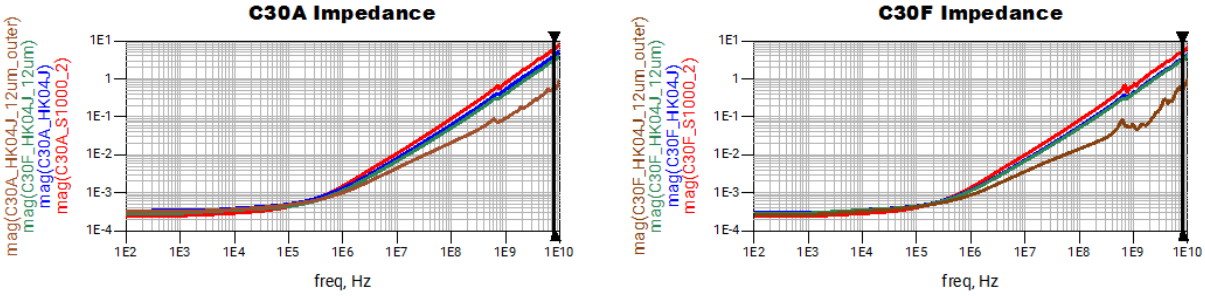


C14 Loop Inductance (pH)

name	L_pH_C14 freq=7.943 GHz
mag(C14_S1000_2)	89
mag(C14_HK04J)	54
mag(C14_HK04J_12um)	51
mag(C14_HK04J_12um_outer)	14

C23AA Loop Inductance (pH)

name	L_pH_C23AA freq=7.943 GHz
mag(C23AA_S1000_2)	116
mag(C23AA_HK04J)	79
mag(C23AA_HK04J_12um)	73
mag(C23AA_HK04J_12um_o...	14



C30A Loop Inductance (pH)

name	L_pH_C30A freq=7.943 GHz
mag(C30A_S1000_2)	124
mag(C30A_HK04J)	82
mag(C30F_HK04J_12um)	61
mag(C30A_HK04J_12um_out...	12

C30F Loop Inductance (pH)

name	L_pH_C30F freq=7.943 GHz
mag(C30F_S1000_2)	105
mag(C30F_HK04J)	67
mag(C30F_HK04J_12um)	61
mag(C30F_HK04J_12um_out...	10

Figure 8 - Loop Inductance from Load Board GaN FET Cells to Select Power Board Capacitors

The Interra® HK04J material offers better loop inductances all around. However, loop inductance is dramatically improved when the thinner, 12 µm material is located only on the outer layers of the stackup, even with the decoupling capacitors and the load on opposite sides of the PCB. The 12 µm Interra® HK04J offers an 84-90% reduction in loop inductances, making the path between the decoupling capacitors nearly transparent. This allows the bypass charge of each of the decoupling capacitors to be delivered with minimal delay and a lower L di/dt noise ripple. These results clearly show that the optimal stackup placement of the Interra® HK04J material is at the very top and bottom and directly between power and ground planes.

A particularly interesting observation here is how much the loop inductance is improved at these capacitors that are located directly beneath the load, given that the inductance improvement was made in the horizontal direction. That is, we did not reduce inductance in the vertical direction by reducing height (the Interra® HK04J_12um_outer stackup is thicker than the Interra® HK04J_25um and Interra® HK04J_12um), adding more vias, or spacing the power and ground vias closer together. The improvement was made in the current loops that travel in the horizontal directions.

The full PDN impedance of the combined power and load boards was assessed using measurement-based models for the capacitors listed in Table 4. These components were pre-selected and not further optimized, as their influence is limited to a region of the PDN outside the primary scope of this study. While the simulation encompasses the entire path from power board to load board, the analysis focuses specifically on the region where the load board's performance is impacted.

Table 4 - PDN Capacitors

Part Number	Capacitance	Package	Quantity
GRM155R71H104KE14D	100 nF	0402	1
GRM188C80J226ME15D	22 uF	0603	258
EEF-LX0E471R-F_CAPM	470 uF	7343	32

Figure 9 shows the impedance response, the Q derived from the impedance group delay, and the phase margin determined by the Q at each significant peak in impedance. The Q and phase margin were calculated using NISM, which has been well-demonstrated in [4].

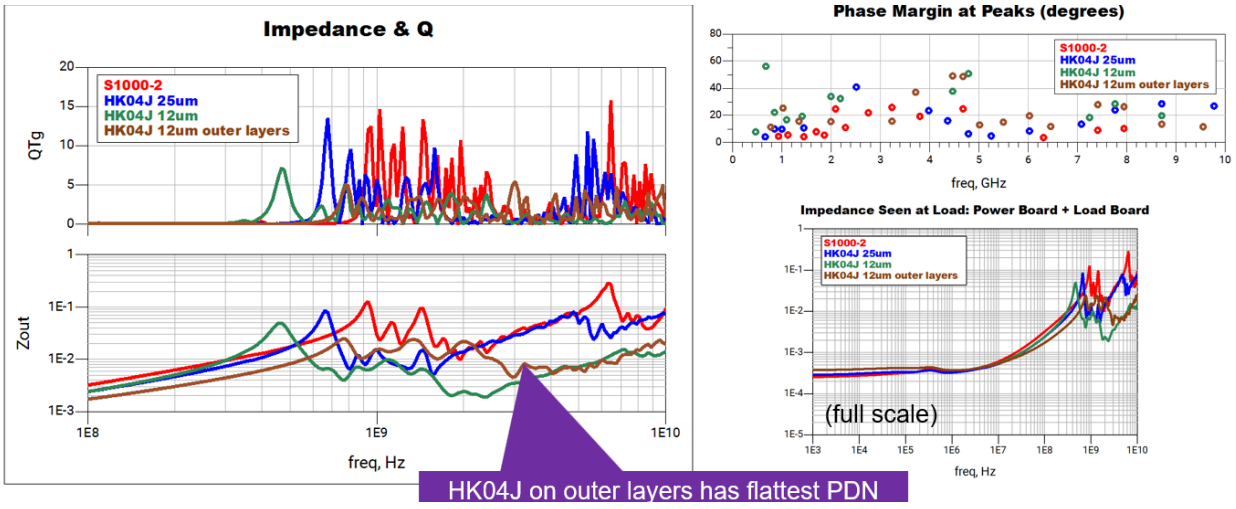


Figure 9 - Full PDN Impedance, Q, and Phase Margin at Impedance Peaks of Combined Power Board and Load Board

The Interra® HK04J configurations show good improvement in reducing the impedance peaks compared to the standard S1000-2 material. The 25 µm Interra® HK04J stackup reduced the peaks of the S1000-2 material, but also shifted them to slightly lower frequencies, which would require larger capacitance values to reduce them. The 12 µm Interra® HK04J stackup reduced the peaks further, but shifted the first peak (the intersection of the VRM control loop and decoupling capacitors) even lower in frequency. The 12 µm Interra® HK04J on just the outer layers shows the best impedance performance, with the flattest impedance response across all stackups.

To maintain a stable phase margin above 30°, the quality factor (Q) should ideally remain below 2 [4]. While all current PDN configurations exhibit resonance peaks exceeding this threshold, this is primarily due to the omission of a die model in the simulation. In a physical application, the Cdie for an ASIC of this scale would provide significant damping for the majority of peaks above 100 MHz. Despite the absence of this damping in the model, the Interra® HK04J 12 µm outer-layer configuration clearly outperforms the alternatives, requiring the fewest design adjustments while offering the superior large-signal transient response. This large-signal step response will be shown in the figures that follow.

b. Simulated Step Response

The step response to a 2000 A, 1 ns load was simulated on two different PDNs using Harmonic Balance to solve for the steady-state operation in the frequency domain, given the known harmonics of a single 2000 A step response. The simulation runs the power board PDN EM S-parameter model, the load board PDN EM S-parameter model, and the dynamic load in less than 5 minutes. The harmonic balance contains the 1 MHz VRM switching frequency tone and 1024 of its harmonics to ensure the PDN is excited out to 1 GHz. The VRM was modeled as an ideal 1 V DC source. While a Sandler State-Space Average Model (SSAM) [2] would provide higher fidelity for both large- and small-signal responses (as established in previous works [2, 5]), the specific VRM parameters required to implement such a model were unavailable at the time of simulation. Regardless, this simplification is justified as the study focuses on PDN behavior at frequencies well beyond the VRM's control loop bandwidth, a regime where the influence of the control loop model is negligible.

These simulation setups are shown in Figures 10 and 11 below. The frequency-domain data are then transformed into the time domain, and the steady-state results are shown in Figure 12.

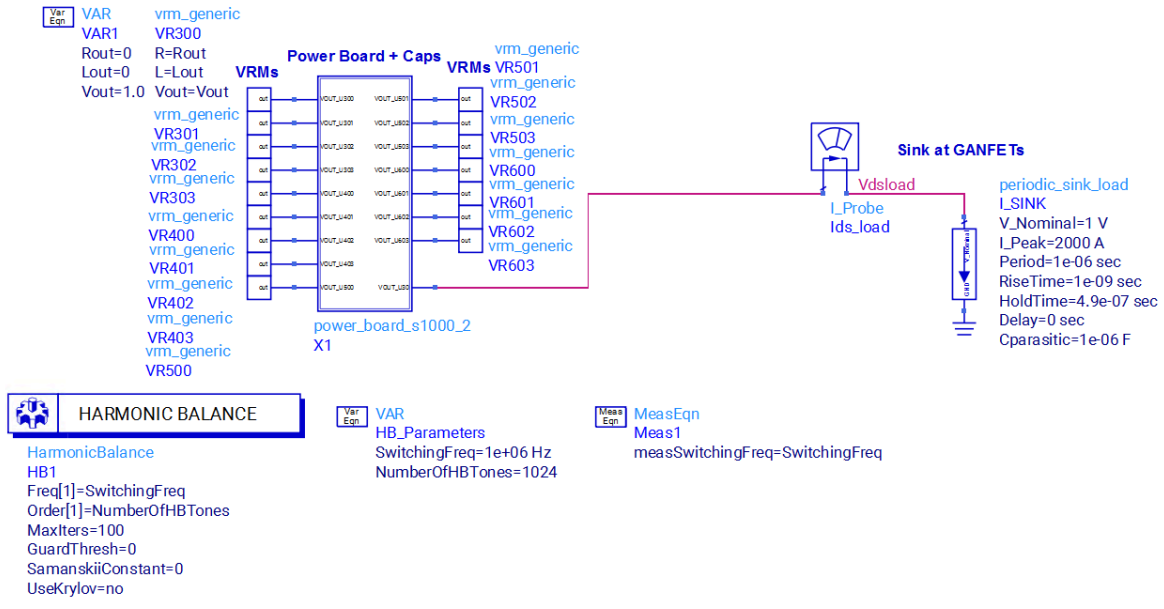


Figure 10 - Simulation Setup - Power Board Only PDN - 2000A, 1ns Step Response

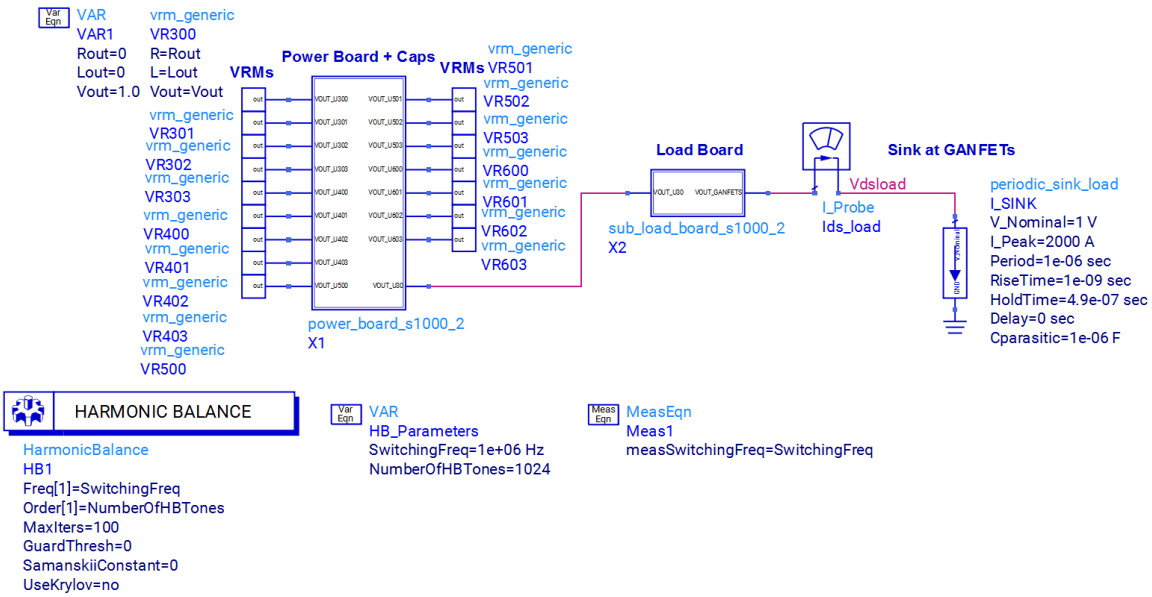


Figure 11 - Simulation Setup - Power Board + Load Board PDN - 2000 A, 1 ns Step Response

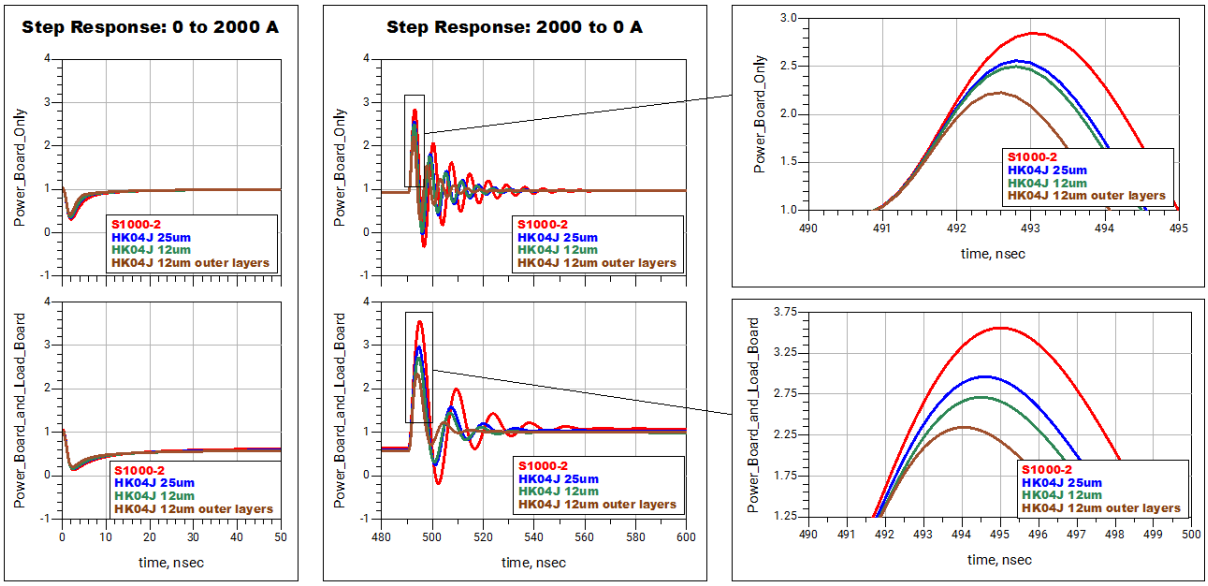


Figure 12 - Simulation Results - 2000 A, 1 ns Step Response with and without the Load Board

Excessive voltage responses are observed and can be explained by the 1 ns step falling in the unstable 700 MHz to 2 GHz region containing multiple peaks with high Qs on all 4 stackups. As expected, we see significant improvement with the embedded capacitor materials compared to the baseline S1000-2 material, as listed in Tables 5 and 6. The Interra® HK04J 12 µm on the outer layers stackup performs best due to its flat impedance response.

Table 5 - Power Board Only 2000 A Step Response Results

	Vmin	**Vmax**	**Vpp**	**f osc.**
S1000_2	-0.331 V	2.846 V	3.176 V	139 MHz
Interra® HK04J_25µm	-0.050 V (-21%)	2.559 V (-10%)	2.608 V (-18%)	156 MHz
Interra® HK04J_12µm	0.022 V (-27%)	2.500 V (-12%)	2.477 V (-22%)	161 MHz
Interra® HK04J_12µm_outer	0.277 V (-47%)	2.226 V (-22%)	1.948 V (-39%)	200 MHz

Table 6 - Power Board & Load Board 2000 A Step Response Results

	Vmin	**Vmax**	**Vpp**	**f osc.**
S1000_2	-0.180 V	3.561 V	3.741 V	69 MHz
Interra® HK04J_25µm	0.158 V (-28%)	2.964 V (-17%)	2.805 V (-25%)	78 MHz
Interra® HK04J_12µm	0.163 V (-29%)	2.711 V (-24%)	2.547 V (-32%)	81 MHz
Interra® HK04J_12µm_outer	0.204 V (-33%)	2.346 V (-34%)	2.142 V (-43%)	94 MHz

The simulations performed up to this point are based on the test fixtures that were built, and are used to correlate the modeling to measurements. However, a more realistic emulation of an ASIC load includes the on-die capacitance (Cdie) and effective resistance to the capacitance (Rdie). Depending on the size of the ASIC, a small ASIC's on-die capacitance typically attenuates the higher-frequency impedance peaks (>500 GHz) and improves performance. An assumption for an ASIC the size of our load board is made, with Rdie = 0.1 mΩ and Cdie = 1 µF. Figure 13 shows the updated simulated impedance response, Q, and phase margin, including this die model, power board, and load board, for each of the 4 stackup configurations.

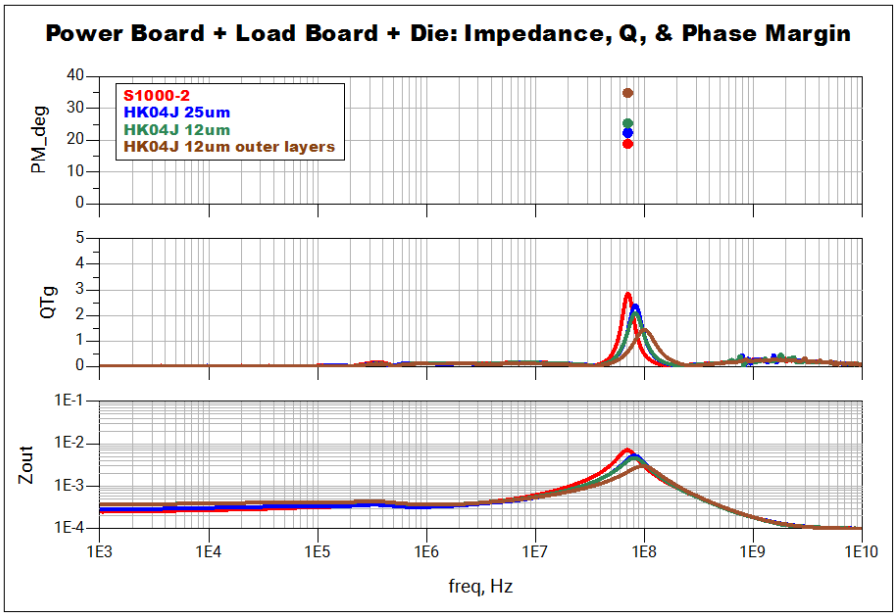


Figure 13 - Impedance, Q, and Phase Margin (degrees) of the Power Board and Load Board with die model

The placement of the 12 µm Interra® HK04J dielectrics on the outer layers provides sufficiently low inductance to significantly improve transient performance. This reduced inductance effectively dampens the Q of the impedance peak formed at the intersection of the die capacitance to a value less than 2. Thus, it can be concluded that the lower total loop inductance of 12 µm Interra® HK04J capacitors on the outer layers allows for the lowest PDN Q response.

Figure 14 shows the simulation setup of the step response of this PDN with this die model, followed by the plotted results in Figure 15 and the summarized results in Table 7.

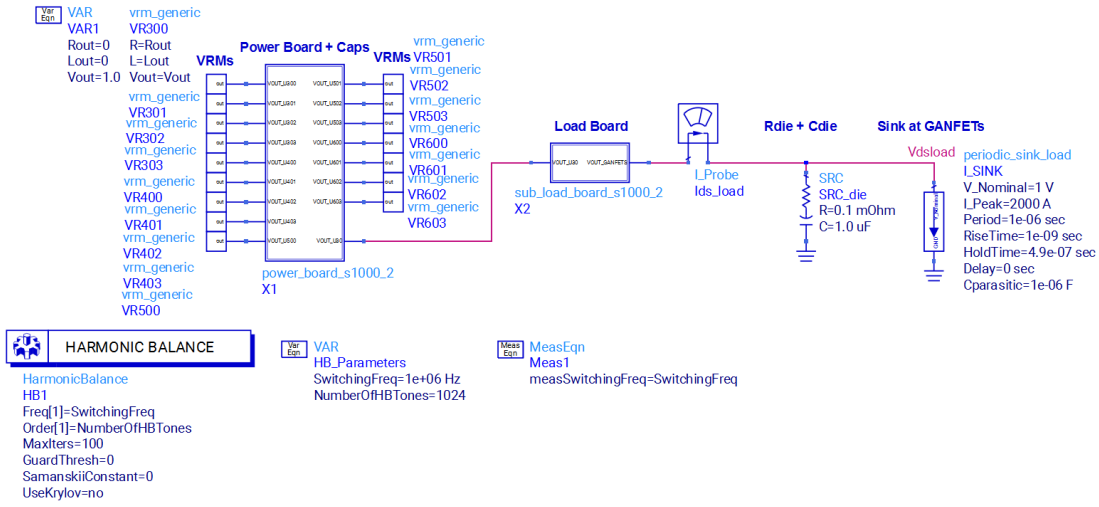


Figure 14 - Simulation Setup - Power Board + Load Board + die model PDN - 2000 A, 1 ns Step Response

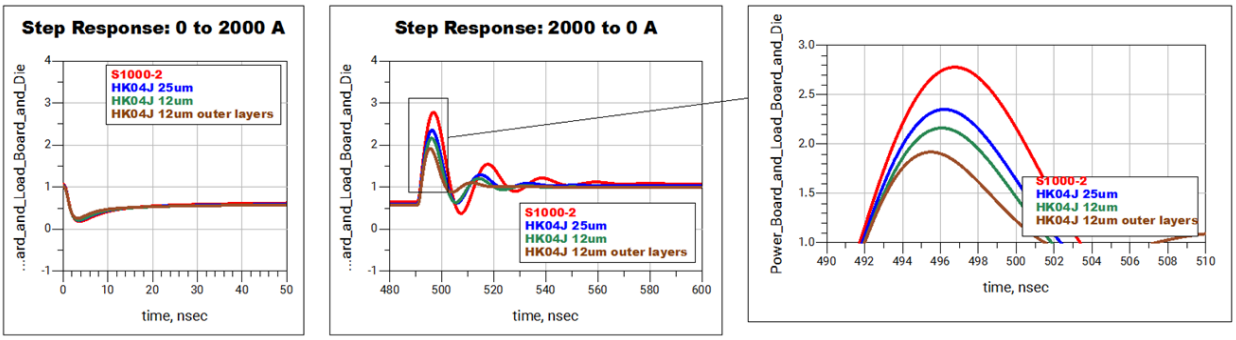


Figure 15 - Simulation Results - Power Board + Load Board + die model PDN - 2000 A, 1 ns Step Response

Table 7 - Power Board & Load Board with Die model 2000 A Step Response Results

	Vmin	**Vmax**	**Vpp**	**f osc.**
S1000_2	0.186 V	2.779 V	2.592 V	48 MHz
Interra® HK04J_25µm	0.209 V (-12%)	2.351 V (-15%)	2.142 V (-17%)	54 MHz
Interra® HK04J_12µm	0.214 V (-15%)	2.162 V (-22%)	1.948 V (-25%)	55 MHz
Interra® HK04J_12µm_outer	0.256 V (-38%)	1.918 V (-31%)	1.662 V (-36%)	63 MHz

The 12 µm Interra® HK04J on the outer-layer stackup has a more stable transient response with minimal ringing. The response with the other stackups that have a Q greater than 2 still ring with a resonant behavior, though with more dampened responses due to the Rdie and Cdie added to the PDN.

c. Simulated Electro-Thermal Performance of 2 oz vs 3 oz Copper

The Interra® HK04J heavy copper options were explored in electro-thermal simulations on the power board. The DC and thermal performance with a 1000 A DC load was run with Interra® HK04J_25um stackup listed in Figure 5 with 2 oz copper layers and compared to the same configuration, but with 3 oz copper layers. For this high-power application, it was assumed for simulation that the ASIC load is fixed at 60 °C as if it were cooled by a liquid flow-through heat sink and that the VRMs performed at 80% efficiency. Figure 16 shows the results of the electro-thermal simulation, and Table 8 summarizes key improvements.

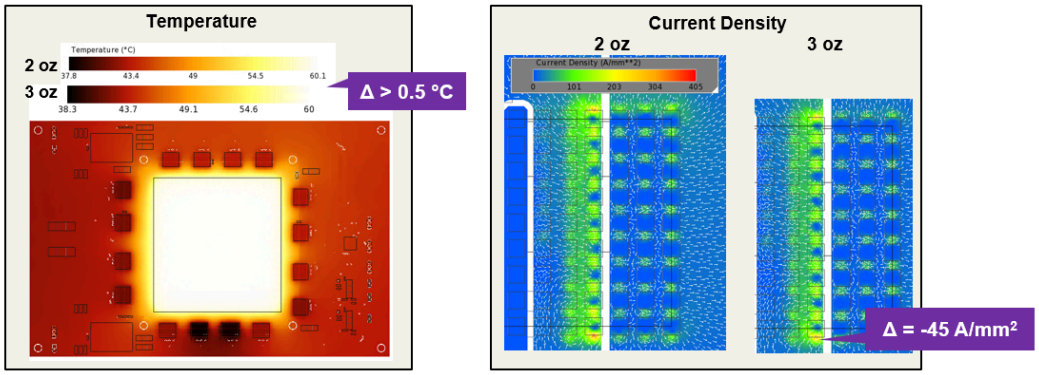


Figure 16 - Electro-Thermal Analysis of the Power Board with Interra® HK04J 2 oz and 3 oz Copper

Table 8 - Summary of Power Board Electro-Thermal Simulation with 2 oz and 3 oz Copper

Parameter	2 oz Cu	3 oz Cu	Improvement
IR Drop	39.9 mV	29.9 mV	25%
VR Phase Current Sharing	-23/+30%	-20/+28%	9%
Max Current Density	405 A/mm^2	360 A/mm^2	11%

Since the load temperature is fixed, we do not see any difference in temperature between the 2 oz and 3 oz copper versions. However, we see thermal improvements in other important ways. First, IR drop improves by 25%, which directly reduces I^2R losses, which means less heat that the cooling system needs to remove. Second, the max current density decreases with 3 oz copper, reducing localized heating within the copper planes. Finally, the lower resistance of the 3 oz copper improves current sharing among voltage regulator phases, which enhances design reliability and longevity.

The impedance response of the Interra® HK04J stackups with 2 oz and 3 oz copper was also evaluated and is shown in Figure 17.

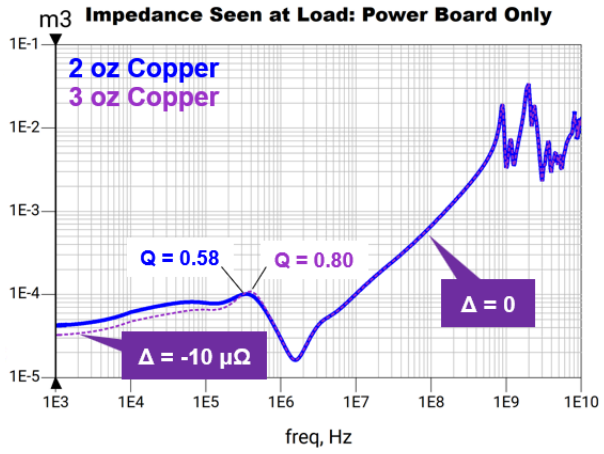


Figure 17 - Power Board Impedance of Interra® HK04J 25 um with 2 oz and 3 oz Copper

The 10 μΩ difference at low frequencies should be considered with the fact that both cases utilized 1 mil plated-through hole vias. Above around 500 kHz, there is no difference in the impedance between the two, implying that there will be no difference in the response to large dynamic loads. In fact, the Q of the peak around 400 kHz increases with the 3 oz copper, since the lower resistance reduces resonant dampening, which suggests that the 3 oz copper could have slightly larger transient responses to dynamic loads.

V. MEASUREMENT RESULTS

The impedance was measured at a test point on the fully assembled load boards, which were mounted to the fully assembled power boards as shown in Figure 18. Note that measuring impedance at this test point is different from measuring the impedance seen by the load using lumped BGA ball and lumped load cell ports.

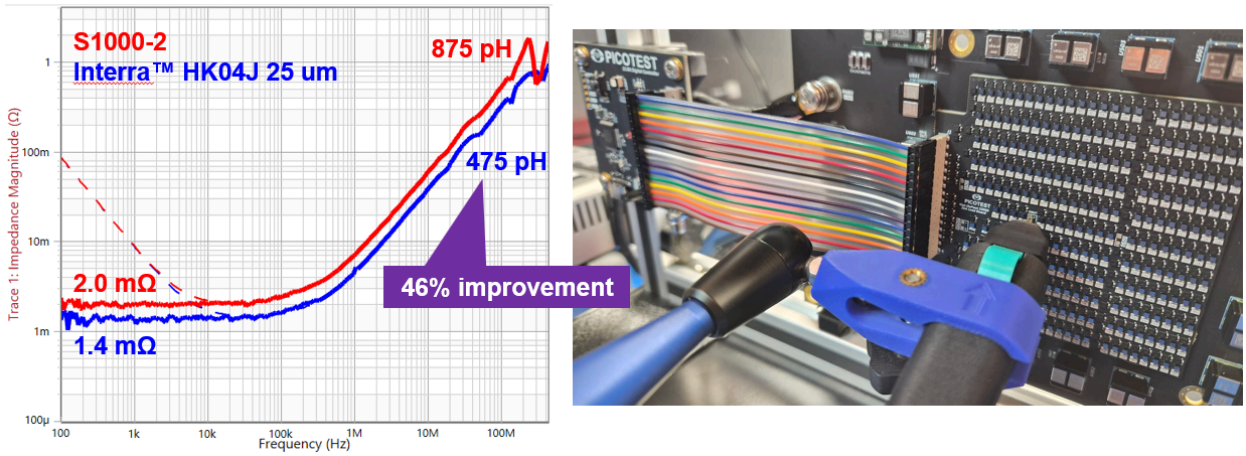


Figure 18 - S1000_2 and Interra® HK04J_25um Impedance Measurements

The measurement is a 2-port shunt-thru impedance measurement using a Picotest P2102A 2-port probe and the Bode 500, 450 MHz VNA. The off measurement (in the dashed traces) shows us just the PDN capacitors and PCB parasitics without the influence of the VRMs, which in this case are very large tantalums. The dashed traces being on top of one another at lower frequencies highlight that the discrete components in both configurations are the same, and the only difference between the two is the stackups.

The 1 mil Interra® HK04J stackup provides 46% less inductance at 100 MHz looking out from the test point. This is a significant enhancement considering the only difference between the two designs is the stackups.

The response to 1000 A amplitude dynamic loads was also measured from the same probe locations shown in Figure 18. The measurement was made with a Picotest P2105A probe connected to a RT-ZISO isolated probe which was isolated from the oscilloscope with a Rohde & Schwarz RT-ZISO isolating probing system in combination with the Picotest J2115A coaxial isolator for the best measurement bandwidth and accuracy. This measurement setup also ensured a maximum CMRR for all measurements

to mitigate the error caused by probe noise and ground bounce in high-current environments [6]. The dynamic load consisted of a waveform pattern with exponential rises and falls, sharp rises and falls (less than 1 ns GaN FET switching time), sine waves, half-amplitude steps, and random excitations as shown in the yellow traces of Figure 20.

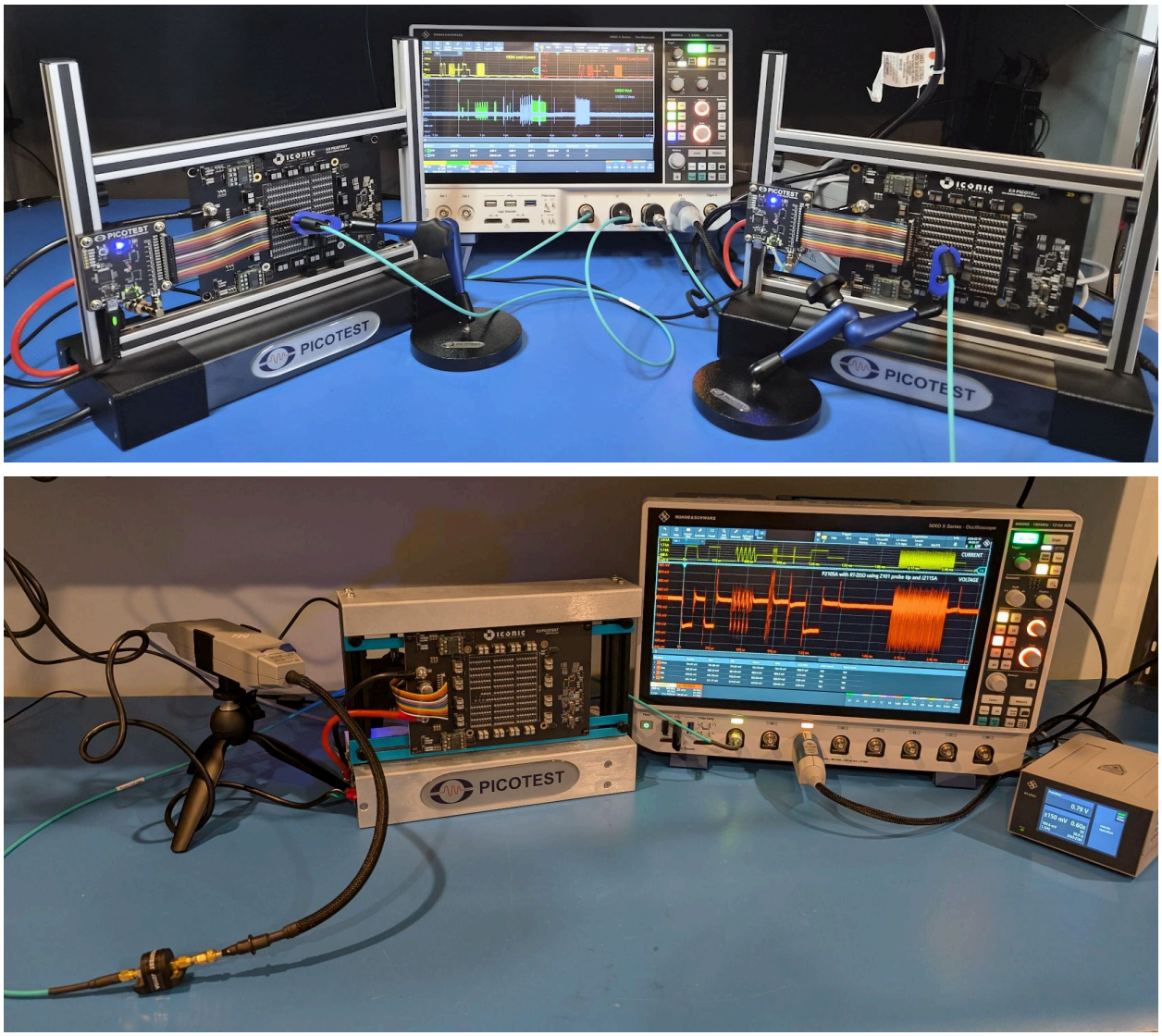


Figure 19 - (TOP) Measurement Setup with MXO4 and Picotest custom Qnity 2000A Test Fixtures, and Isolated Probe RT-ZISO (Not Shown)
(BOT) Measurement Setup with MXO5 Picotest 2000A Test Fixture, P2105A, J2115A, and RT-ZISO Isolated Probing System

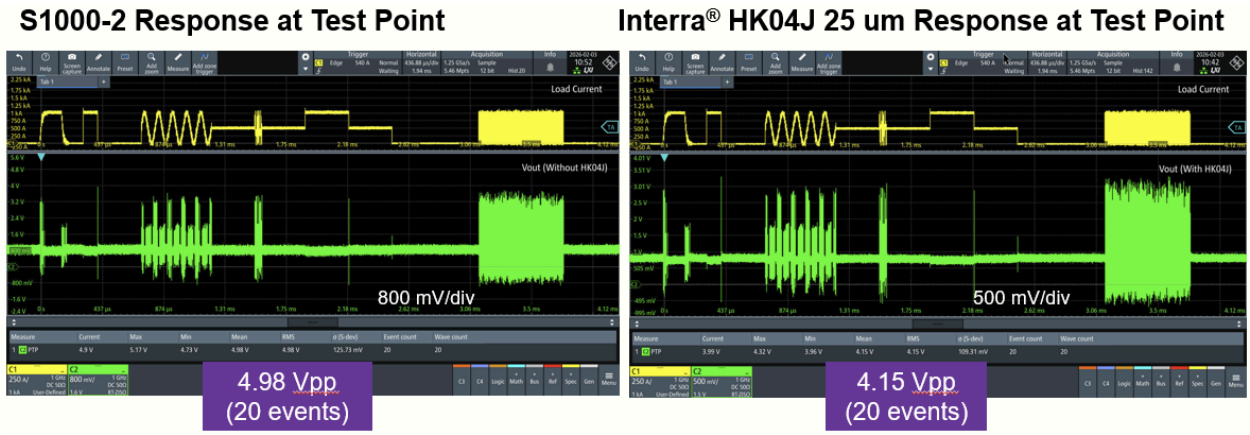


Figure 20 - Measured Voltage Responses to 1000 A Dynamic Loads (Yellow/top: Current, Green/bottom: Voltage)

These results follow the simulation trend that the Interra® HK04J performs better than the S1000-2 stackup. The peak-to-peak response, as averaged across 20 samples, is 4.98 V with the S1000-2 and 830 mV less at 4.15 V with the Interra® HK04J. This is a significant 17% improvement for only reducing the thickness between power and ground planes by 1 mil.

The measured falling step response that was evaluated in simulation is shown in Figure 21. The Interra® HK04J shows a 1 V, or 20%, improvement over the S1000-2 for this measurement with a sample size of 1.

Figure 21 - Measured 1000 A to 0 A Step Response (Yellow/top: Current, Green/bottom: Voltage)

These step responses are much larger than what was simulated for the 2000 A to 0 A steps in current. The simulation was revisited to better match the characteristics of the physical test fixture. The output voltage was corrected from 1 V to 0.8 V. The fall time of the current step was set from 1 ns to 0.5 ns, and the amplitude was adjusted from 2000 A to 1000 A. The parasitic load capacitance was reduced from 1 µF to 100 nF to better approximate the effective capacitance of the combined GaN FET output capacitance. Most importantly, the probe point was moved from directly at the load at the lumped GaN FET cells, to the test point on the load board.

These changes are shown in the schematic representation in Figure 22, the new simulation results show much better correlation to the measurements in Figure 23, and they are summarized in Table 9.

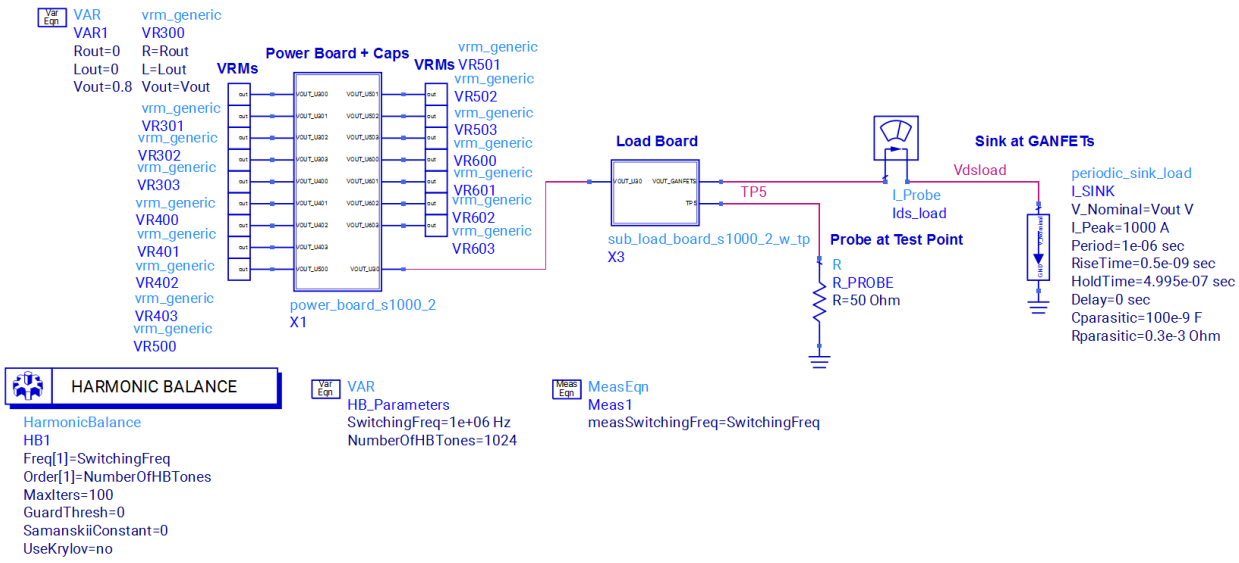


Figure 22 - Updated Simulation Schematic

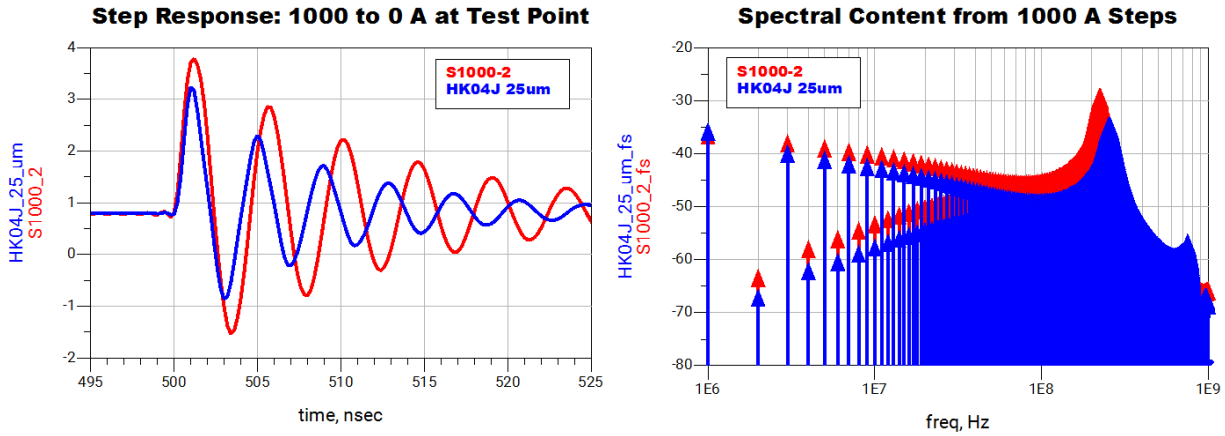


Figure 23 - Updated Simulation Results

Table 9 - Summary of Measured and Simulated Voltage Responses to 1000 A to 0 A Load Step

	Simulated Response	**Measured Response**
S1000_2	5.320 Vpp	5.13 Vpp
Interra® HK04J_25um	4.103 Vpp	4.15 Vpp

VI. EMI PERFORMANCE

Conducted and radiated EMI are also important real-world challenges when designing electronic hardware. Often, it is left until after hardware is built to assess the potential EMI problems; however, simulating early and understanding the design trade-offs can avoid late design failures. The source of radiated EMI is from the surface current densities, so one can look at current densities on the top or bottom of a PCB to look for high di/dt current densities that can radiate. The current density in Figure 23 below is generated by using the simulated electrical data set from the end-to-end PI schematic in Figure 21. This includes a 2000 Amp dynamic load pulling current all the way from the 1 Volt power board supplies through the power board and up into the load board.

The current densities are plotted at 20MHz and show higher current densities for the S1000_2, i.e., more red locations than the Interra® HK04J with the thin 12um outer layers. This is somewhat subjective, since it is really the common-mode currents traveling in the same direction on the power and ground nets that generate the conducted and radiated EMI. However, this visualization of current densities does show how the lower path inductance from the capacitors to the load PCB can spread the currents out, pull more current from capacitors that are farther away, and provide lower overall current densities.

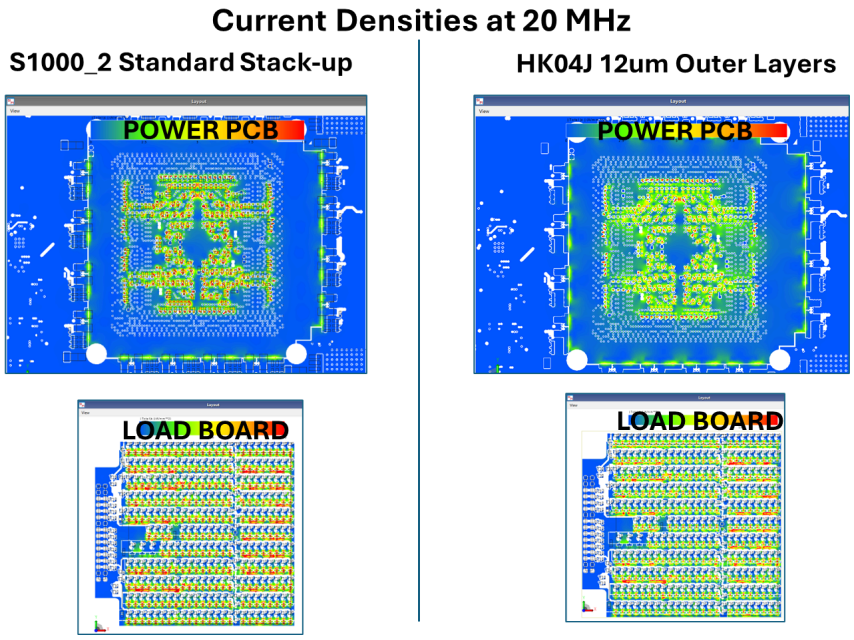


Figure 24 - Current Density Results at 20 MHz Excitation

Typically, conducted EMI is measured at the point where the power connects to a PCB. In this case, it would be the 48V supply. This 48V supply is stepped down to 12V, then to 1V that powers the 2000 Amp load. To simulate conducted EMI at the 48 Volt power connector, the end-to-end PI simulation is run with simple open-loop switch models for the regulators and a switching 2000 Amp step load. The EM simulator generates the Power Board and Load Board with a virtual reference ground plate to enable differential and common-mode measurements between the power and ground nets at the 48 Volt connector. The results are shown in Figure 25 below. This data clearly shows that the Interra® HK04J material, with thin 12 µm layers on the top and bottom of the PCB, can significantly reduce conducted

EMI in the 10 to 100 MHz region. Note that this is the noise at the 48V connector, with a significant amount of the high-frequency step-load noise being filtered by the transfer impedance of the PDN. Here again, we see the benefit of the lower inductance helping to reduce EMI by making the PCB capacitors more effective at higher frequencies and providing more uniform current distribution.

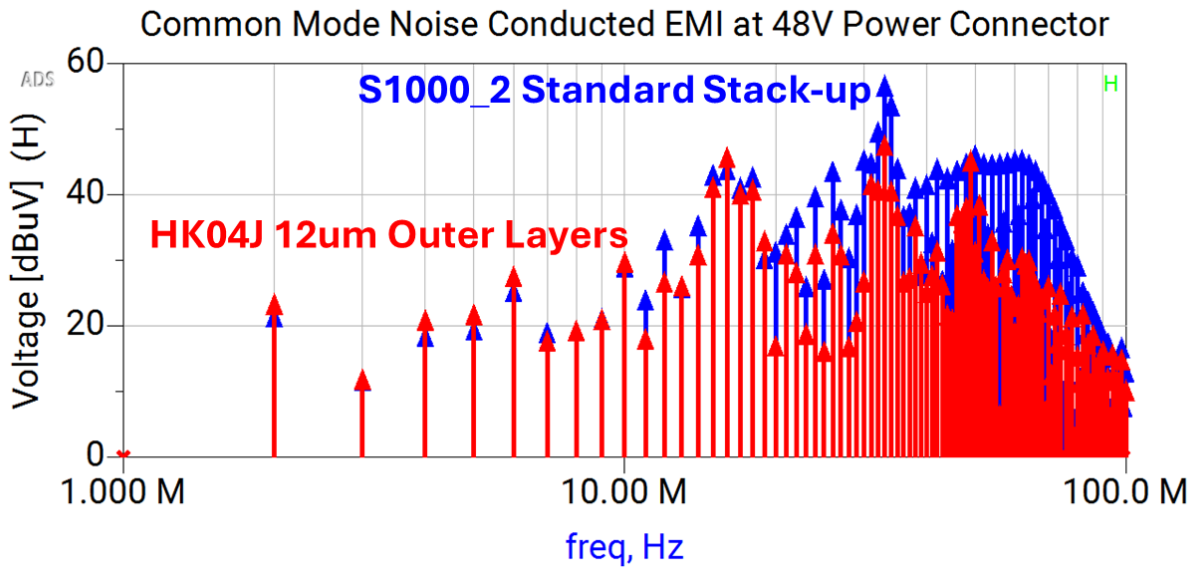


Figure 25 - Conducted EMI Simulation Results at 48V Connector - Interra® HK04J material Outer Layers vs. S1000 Stack-up

VII. CONCLUSIONS AND SUMMARY

This exploration of embedded capacitor materials initially assumed that the added integral capacitance within the stackup would be the primary driver for improved impedance and step-load performance. However, the results demonstrate that the most significant advantage of materials like Interra® HK04J is that their ultra-thin profiles enable a drastic reduction in loop inductance in the stackup. When optimally integrated on the outer layers of a stackup, the material provides significant value to the PDN by minimizing the total loop inductance, which is the primary factor influencing performance in this design. This improvement is clearly reflected in the Q and stability margin analysis using NISM, which confirms a more stable transient response. It is also evident in the performance enhancement demonstrated in the step responses as well as in the 20 MHz current densities and the common mode noise EMI. PCB fabricators have confirmed that positioning the ultra-thin Interra® HK04J material exclusively on the top and bottom layers for the optimal electrical performance provides neither a manufacturing challenge nor benefit over a symmetrical stackup that incorporates multiple ultra-thin layers throughout. Future work will involve the fabrication of this platform with the thin Interra® HK04J material on the outer layers to obtain real-world measurements and validate the correlation between simulated data and physical hardware.

Thick copper planes provide a robust, low-impedance path for power distribution, enabling higher current flow with reduced heating and ensuring stable voltage delivery to sensitive components.

Future research will focus on fabricating 3 oz copper paired with a 12 µm Interra® HK04J dielectric as the P–G layer stack-up. This work will help evaluate how combining heavy copper with an ultra-thin embedded capacitance layer can further improve thermal performance in high-current boards and reduce DCIR drop across the power distribution network.

VIII. ACKNOWLEDGEMENTS

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